RISC Core C400 Datasheet

Summary

This document describes the functionality of the C*CORE C400 platform microprocessor.

C400 series CPU remains 100% backward compatible with the C300 core's instruction set. As the new generation processor, it extends the original 16bit instruction set to a 16bit/32bit mixed instruction set.

Different from C300 family, the C400 processor family is based on 32bit load-store Harvard architecture. C400 is a 8-stage pipeline cpu which doubles the maximum clock frequency of C300. Its target frequency is about 500MHz in 65nm general process.

The C400 processor family also changes the external bus protocol from the C300 local bus to AXI bus.

Obviously, the user will benefit from it when they want to replace the other core with C400 since AXI bus is more popular and powerful. The bus architecture is also suitable for multicore implementation.

The C400 processor also support fast, low-latency bus access through optional Cache, MMU and tightly coupled memories.

C405, C410, CS420 and C440 are based on C400 processor. For die size/power optimization, C405 has the minimum cache configuration and has no MMU. C440 implements the complete features of C400 and has the maximum cache and TCM configuration. C410 is a shrinked version of C440 with the smaller cache and without TCM. CS420 extends the security functionality based on C410.

Features

The main features of the C400 are as follows:

- Support 16/32bit mixed C2 instruction set. Backward compatible with C300 instruction set (C1).
- 32-bit load-store Harvard Architecture
- 16-entry 32-bit general-purpose register file
- An 8-stage pipeline, hidden from application software
- 14-entry dedicated alternate register file
- Branch prediction support
- Internal coprocessor support by extended 32-bit instructions

- Separated 64-bit AXI bus for program and data
- Cache/MMU support
- Tightly-Coupled Memory (Optional)
- DMA support (Optional)
- JTAG-based debug

C400 has eight pipeline stages. Figure 1-1 shows the pipeline stages.

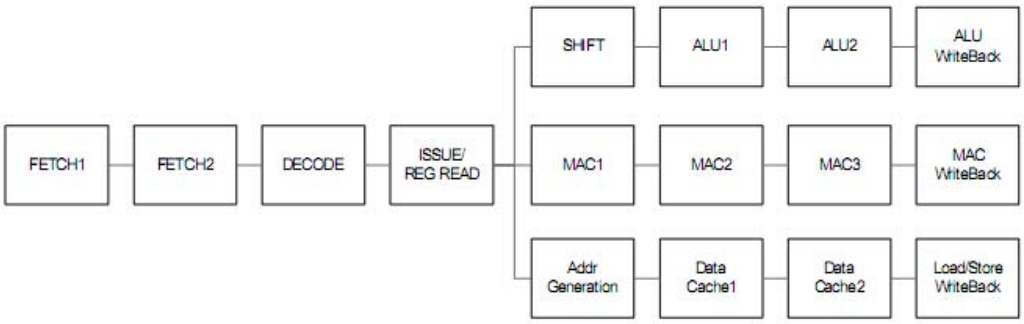

Figure 1-1 C400 Pipeline Stages

The pipeline stages are:

- FETCH1 First stage of instruction fetch where address is issued to memory and data returns from memory
- FETCH2 Second stage of instruction fetches and branch prediction.
- DECODE Instruction decode.
- ISSUE/REG READ Register read and instruction issue.
- SHIFT Shifter stage.
- ALU1 1st integer operation calculation.
- ALU2 2nd integer operation calculation.
- WriteBack Write back of data from the ALU, Multiply or Load Store Unit.
- MAC1 First stage of the multiply-accumulate pipeline.
- MAC2 Second stage of the multiply-accumulate pipeline.
- MAC3 Third stage of the multiply-accumulate pipeline.
- Addr Generation Address generation stage.
- Data Cache1 First stage of data cache access.
- Data Cache2 Second stage of data cache access.

*To obtain more information about the C400 or other C*Core™ products, please contact the C*Core Technology Co., Ltd. by phone: 0512-68091377, email: support@china-core.com or web: http://www.china-core.com.*