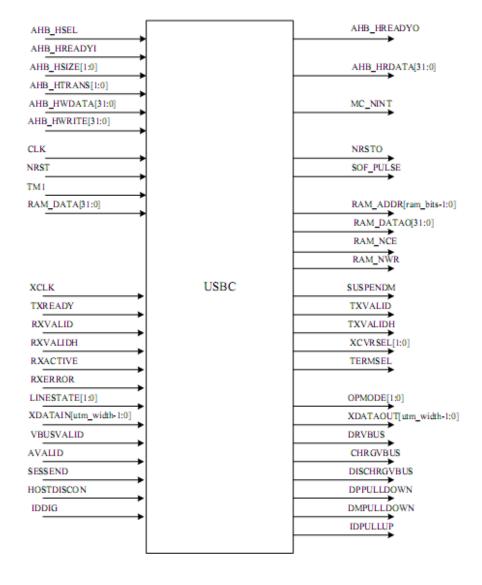
USBC USB Controller Module

Summary

The USBC operates as the USB2.0 host/peripheral USB controller with AMBA AHB compatible interface. It complies with the USB2.0 standard for high-speed and full-speed, also supports Suspend and Resume signaling. It is configurable for different transmit and receive endpoints base on different requirement, and supports four types USB transfer.



USBC Interface Diagram



Features

- ➤ Complies with USB 2.0 standard, also support USB OTG.
- > Supports point-to-point communications with one high-, full- or low-speed device
- Support Control, Bulk, Interrupt, Isochronous transfer
- ➤ Configurable for up to 15 additional transmit endpoints and up to 15 additional Receive endpoints
- ➤ Configurable FIFOs
- ➤ High-level AMBA AHB-compatible interface
- Synchronous RAM interface for FIFOs
- Encodes, decodes, checks and directs all USB packets sent and received
- Suspend and resume signaling
- ➤ Soft connect/disconnect option

Performance and Characteristics

 \triangleright Die Size: 0.76 mm²

Process: 0.18μm (WCS, 1.62V, 120°)

Deliverables

- Verilog HDL source code
- Verilog HDL test pattern
- Documentation

Availability

> Q2, 2006

To obtain more information about the USBC or other C^*Core^{TM} products, please contact the C^*Core Technology Co., Ltd. by phone: 0512-68091375, email: $\underline{support@china-core.com}$ or web: $\underline{http://www.china-core.com}$. C^*Core^{TM} is a trade mark of C^*Core Co., Ltd.

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