

CCFC2017BC Microcontroller Data Sheet(V1.4)

Features

- Single issue, 32-bit CPU core complex (C3007)
 - Compliant with the Power Architecture® technology embedded category
 - Enhanced instruction set allowing variable length encoding (VLE) for code size footprint reduction. With the optional encoding of mixed 16-bit and 32-bit instructions, it is possible to achieve significant code size footprint reduction.
- Up to 2.5 MB on-chip code flash memory supported with the flash memory controller
- 512 KB on-chip data flash memory with ECC
- Up to 416 KB on-chip SRAM
- Memory protection unit (MPU) with 8 region descriptors and 32-byte region granularity on certain family members (Refer to [Table 1](#) for details.)
- Interrupt controller (INTC) capable of handling 363 selectable-priority interrupt sources
- Frequency modulated phase-locked loop (FMPLL)
- Crossbar switch architecture for concurrent access to peripherals, Flash, or RAM from multiple bus masters
- 64-channel eDMA controller with multiple transfer request sources using DMA multiplexer
- Boot assist module (BAM) supports internal Flash programming via a serial link (CAN or SCI)
- Timer supports I/O channels providing a range of 16-bit input capture, output compare, and pulse width modulation functions (eMIOS)
- 2 analog-to-digital converters (ADC): one 10-bit and one 12-bit
- Cross Trigger Unit to enable synchronization of ADC conversions with a timer event from the eMIOS or PIT
- Up to 9 serial peripheral interface (DSPI) modules, microsecond downlink available on dsp_i_8.
- Up to 12 serial communication interface (LINFlex) modules
- Up to 8 enhanced full CAN (FlexCAN) modules with configurable buffers, each can interface compatible with canfd interface.
- 4 inter-integrated circuit (I²C) interface module
- Up to 149 configurable general purpose pins supporting input and output operations (package dependent)
- Real-Time Counter (RTC)
- Clock source from internal 128 kHz or 16 MHz oscillator supporting autonomous wakeup with 1 ms resolution with maximum timeout of 2 seconds
- Optional support for RTC with clock source from external 32 kHz crystal oscillator, supporting wakeup with 1 sec resolution and maximum timeout of 1 hour
- Up to 8 periodic interrupt timers (PIT) with 32-bit counter resolution
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 Class Two Plus
- Device/board boundary scan testing supported per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)
- On-chip voltage regulator (VREG) for regulation of input supply for all internal levels
- HSM support RSA up to 3072 with 10 general purpose AES keys and 4 general RSA keys.

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1 Introduction

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device.

1.1 Description

This family of 32-bit system-on-chip (SoC) microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding family of automotive-focused products designed to address the next wave of body electronics applications within the vehicle.

The advanced and cost-efficient C3007 host processor core of this automotive controller family complies with the Power Architecture technology and only implements the VLE (variable-length encoding) APU (Auxiliary Processor Unit), providing improved code density. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

Table 1. CCFC2017BC family comparison

NO.	Version Function	CCFC2017BC90L7	CCFC2017BC90L5	CCFC2017BC90L3
	1	CPU	C3007(compatible with e200z7)	C3007(compatible with e200z7)
2	Frequence	300Mhz	300Mhz	300Mhz
3	CFLASH	2.5M	2.5M	2.5M
4	DFLASH	512K	512K	512K
5	SRAM	416K	416K	416K
6	PLL	FMPLL	FMPLL	FMPLL
7	eDMA	64	64	64
8	FlexCAN	8 (CanFD)	8 (CanFD)	8 (CanFD)
9	DSPI	9	7	5
10	LINFlex	14	12	7
11	eMIOS	64	64	37
12	ADC	10bit+12bit/53ch	10bit+12bit/39ch	10bit+12bit/33ch
13	eTPU	second generation eTPU	second generation eTPU	second generation eTPU
14	PIT/STM/SWT	8/4/1	8/4/1	8/4/1
15	I2C	4	2	2
16	GPIO	149	121	79
17	HSM	1	1	1
18	Package	LQFP176	LQFP144	LQFP100
19	Pin	MPC5607*/ SPC560B64L7*	MPC5607*/ SPC560B64L5*	MPC5607*/ SPC560B64L3*
20	Replaceability	CYT2B98*/ SPC5744B*/ R7F7016483*	CYT2B98*/ SPC5744B*/ R7F7016483*	CYT2B98*/ SPC5744B*/ R7F7016483*
21	Reliability	AEC-Q100	AEC-Q100	AEC-Q100
22	Functional Safety	ASIL-B	ASIL-B	ASIL-B

2 Block diagram

Figure 1 shows a top-level block diagram of the CCFC2017BC.

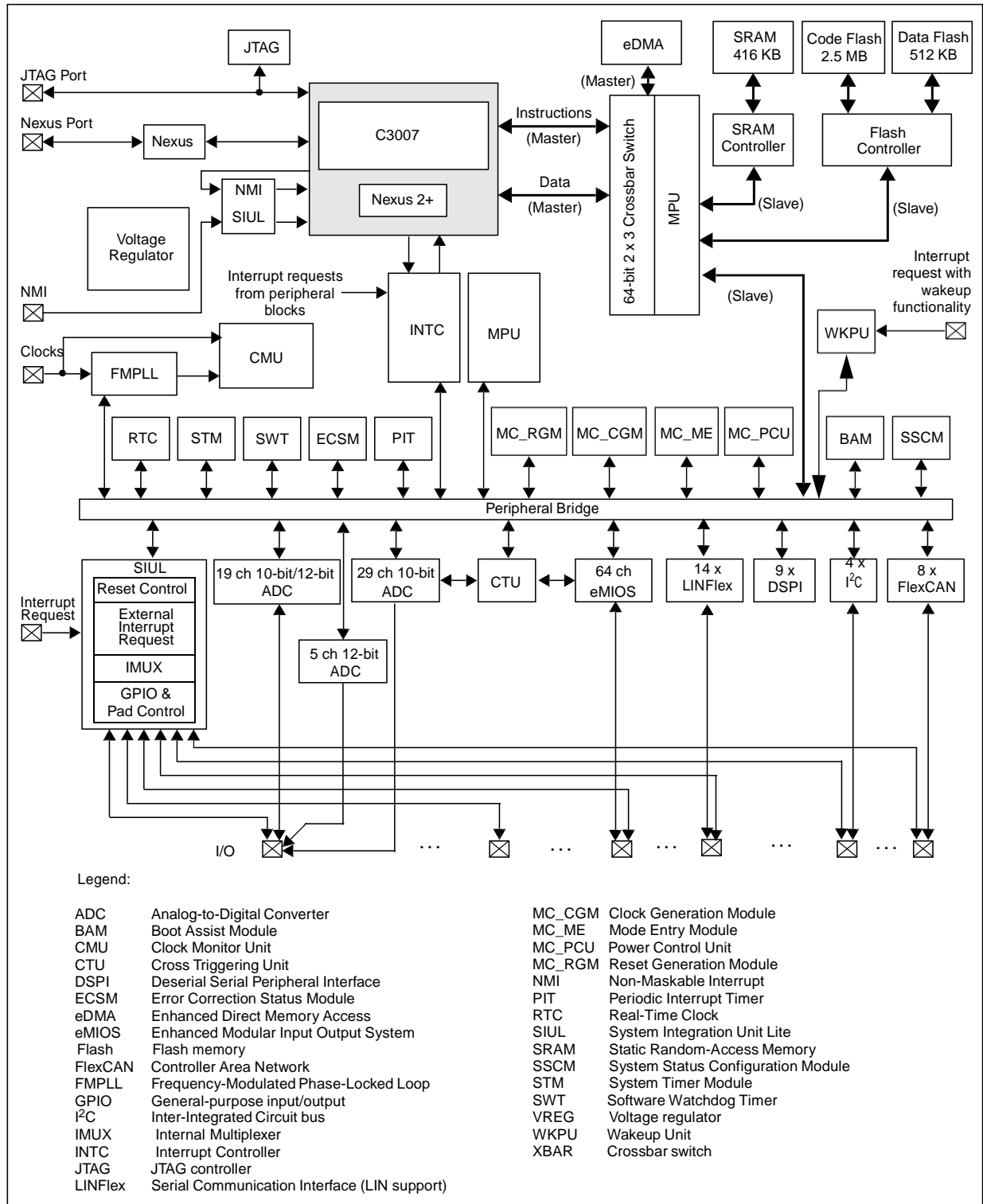


Figure 1. CCFC2017BC block diagram

Table 2 summarizes the functions of the blocks present on the CCFC2017BC.

Table 2. CCFC2017BC series block summary

Block	Function
Analog-to-digital converter (ADC)	Converts analog voltages to digital values
Boot assist module (BAM)	A block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Clock monitor unit (CMU)	Monitors clock source (internal and external) integrity
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Crossbar switch (XBAR)	Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Enhanced direct memory access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via "n" programmable channels
Enhanced modular input output system (eMIOS)	Provides the functionality to generate or measure events
Error correction status module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexCAN (controller area network)	Supports the standard CAN communications protocol
Frequency-modulated phase-locked loop (FMPDLL)	Generates high-speed system clocks and supports programmable frequency modulation
Inter-integrated circuit (I ² C) bus	Two-wire bidirectional serial bus that provides a simple and efficient method of data exchange between devices
Internal multiplexer (IMUX) SIU subblock	Allows flexible mapping of peripheral interface on the different pins of the device
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller (JTAGC)	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Memory protection unit (MPU)	Provides hardware access control for all memory references generated in a device
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and modetransition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Non-maskable interrupt (NMI)	Handles external events that must produce an immediate response, such as power down detection

Block diagram**Table 2. CCFC2017BC series block summary (continued)**

Block	Function
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called "power domains" which are controlled by the PCU
Real-time counter (RTC)	A free running counter used for time keeping applications, the RTC can be configured to generate an interrupt at a predefined interval independent of the mode of operation (run mode or low-power mode)
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System integration unit lite (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status and configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR (Automotive Open System Architecture) and operating system tasks
Software watchdog timer (SWT)	Provides protection from runaway code
Wakeup unit (WKPU)	The wakeup unit supports up to 27 external sources that can generate interrupts or wakeup events, of which 1 can cause non-maskable interrupt requests or wakeup events.

3 Package pinouts and signal descriptions

3.1 Package pinouts

The available LQFP pinouts and the ballmap are provided in the following figures. For pin signal descriptions, please see [Table 5](#).

Figure 2 shows the CCFC2017BC90L3 in the 100 LQFP package.

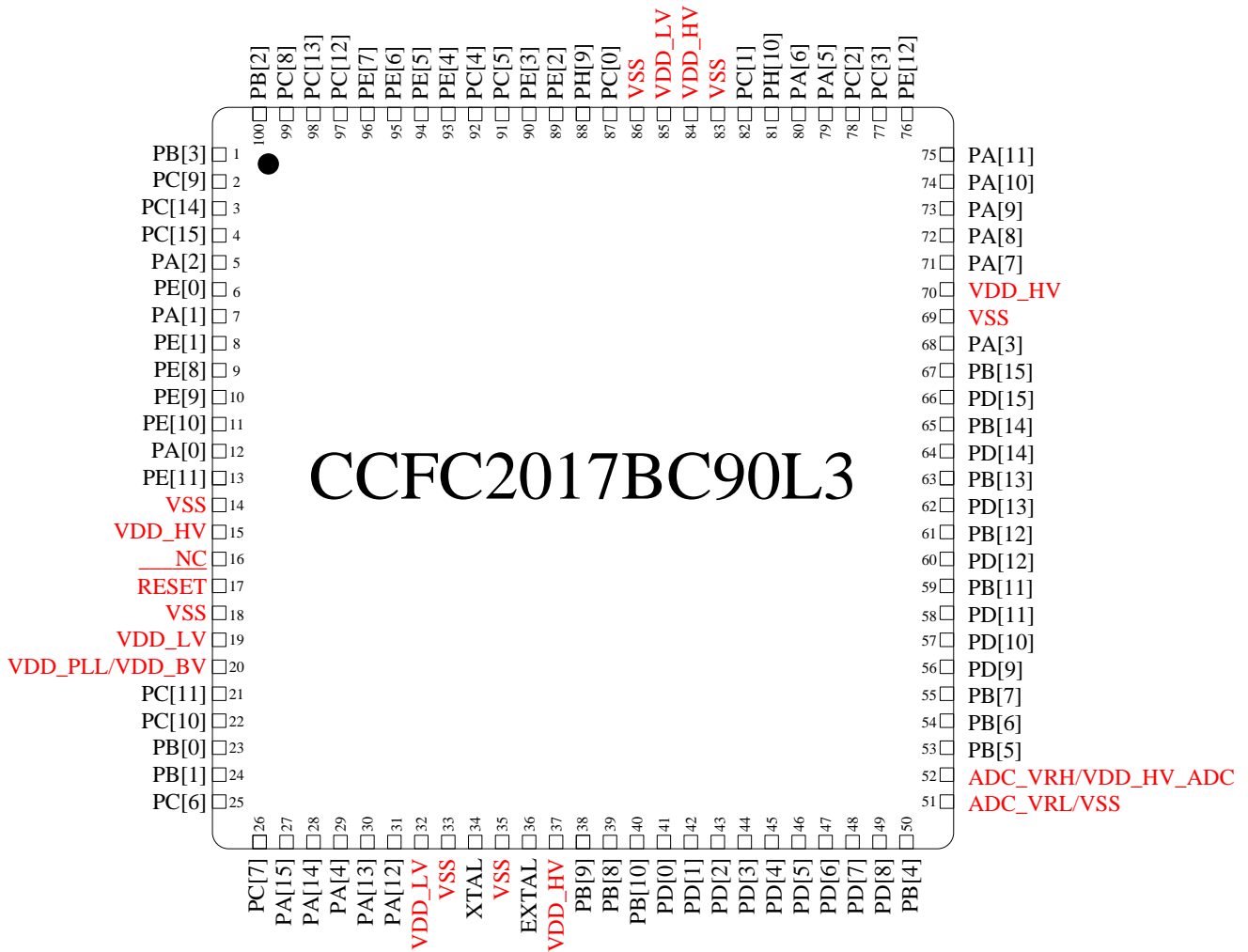


Figure 2. CCFC2017BC90L3 100 LQFP pin configuration

Package pinouts and signal descriptions

Figure 3 shows the CCFC2017BC90L5 in the 144 LQFP package.

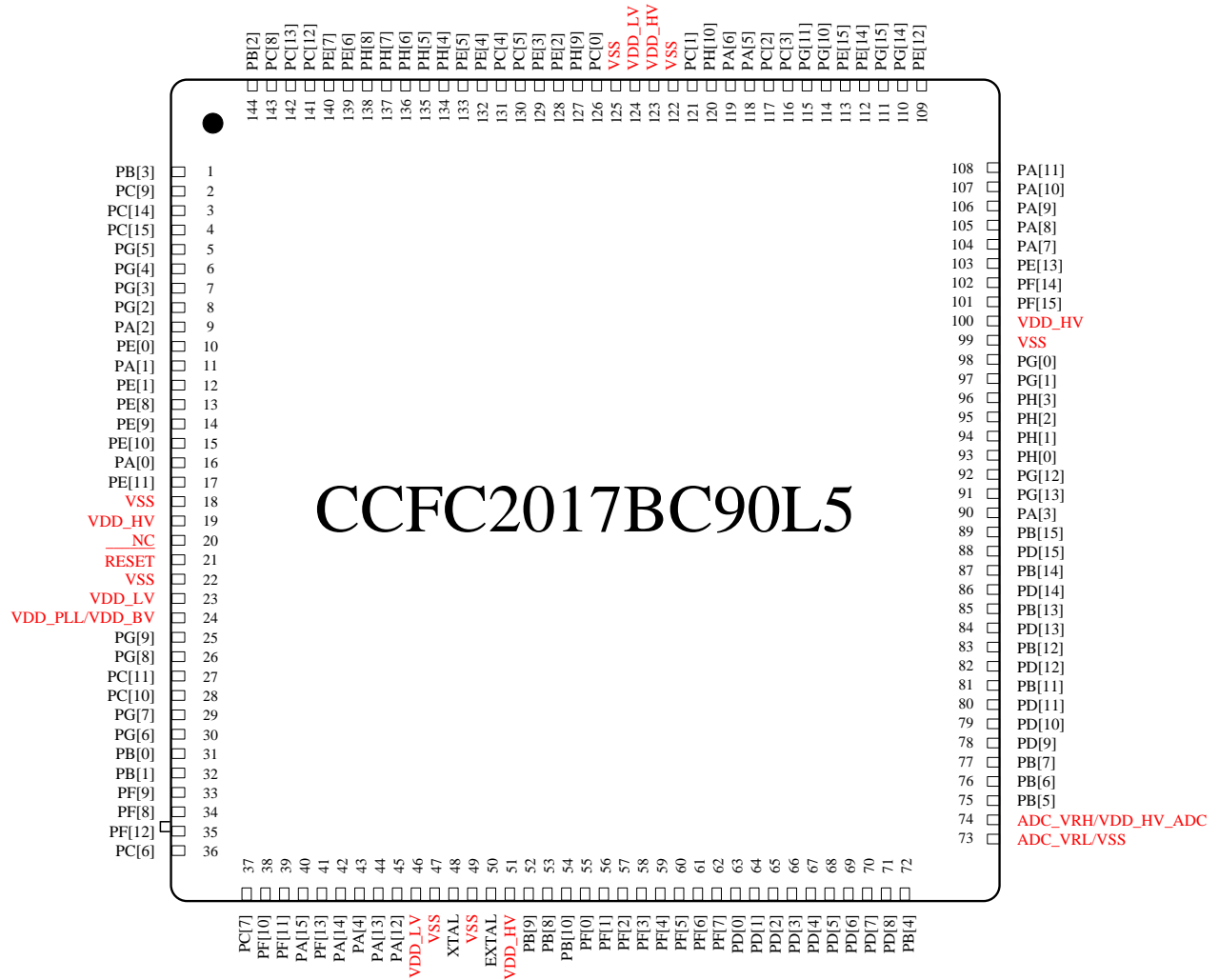


Figure 3. CCFC2017BC90L5 144 LQFP pin configuration

Figure 4 shows the CCFC2017BC90L7 in the 176 LQFP package.

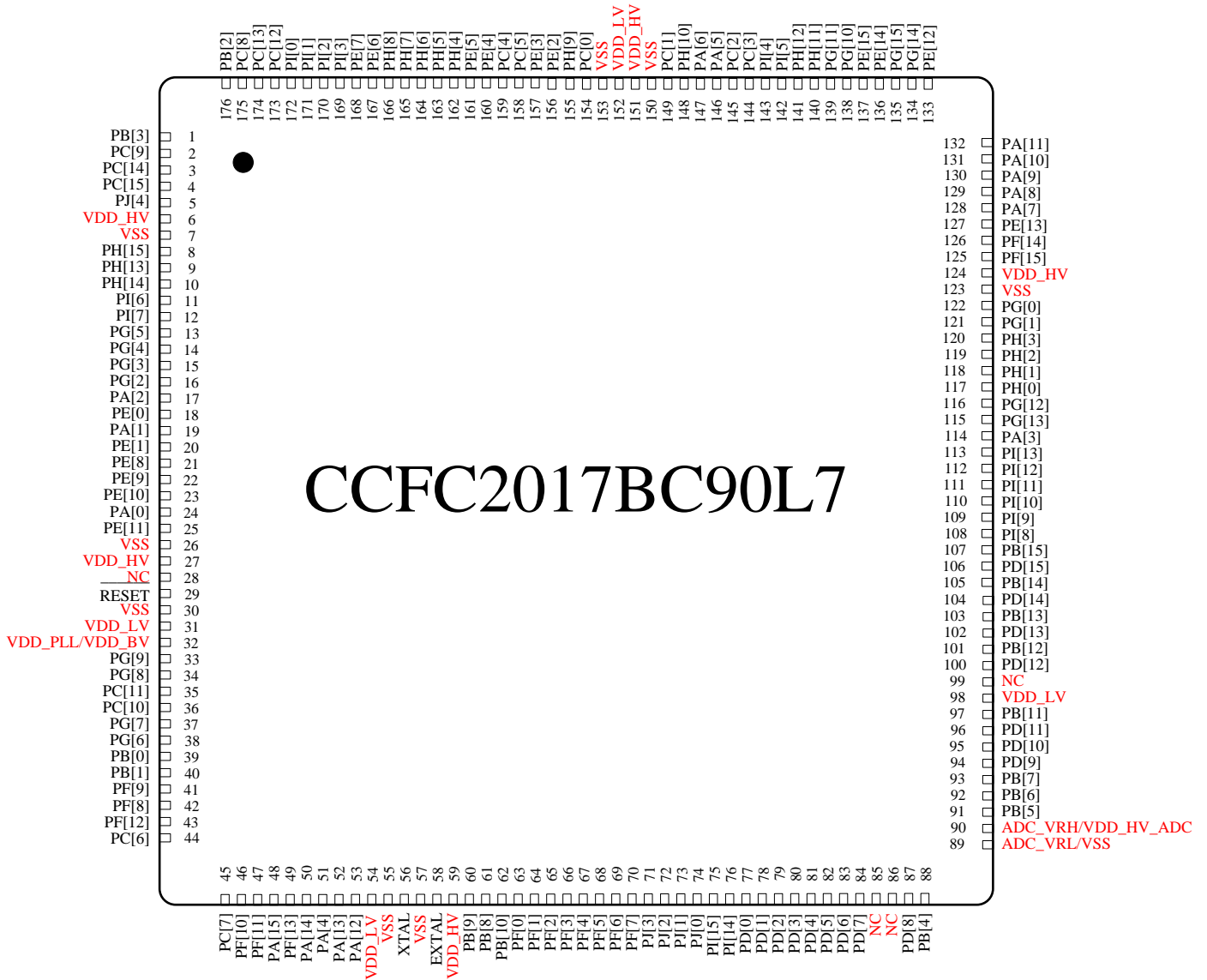


Figure 4 CCFC2017BC90L7 176 LQFP pin configuration

3.2 Pad configuration during reset phases

All pads have a fixed configuration under reset.

During the power-up phase, all pads are forced to tristate.

After power-up phase, all pads are tristate with the following exceptions:

- PA[9] (FAB) is pull-down. Without external strong pull-up the device starts fetching from flash.
- PA[8], PC[0] and PH[9:10] are in input weak pull-up when out of reset.
- RESET pad is driven low by the device till 40 FIRC clock cycles after phase2 completion. Minimum phase3 duration is 40 FIRC cycles.
- Nexus output pads (MDO[n], MCKO, EVTO, MSEO) are forced to output.

3.3 Pad configuration during standby mode exit

Pad configuration (input buffer enable, pull enable) for low-power wakeup pads is controlled by both the SIUL and WKPU modules. During standby exit, all low power pads PA[0,1,2,4,15], PB[1,3,8,9,10]¹, PC[7,9,11], PD[0,1], PE[0,9,11], PF[9,11,13]², PG[3,5,7,9]², PI[1,3]³ are configured according to their respective configuration done in the WKPU module. All other pads will have the same configuration as expected after a reset.

The TDO pad has been moved into the STANDBY domain in order to allow low-power debug handshaking in STANDBY mode. However, no pull-resistor is active on the TDO pad while in STANDBY mode. At this time the pad is configured as an input. When no debugger is connected the TDO pad is floating causing additional current consumption.

To avoid the extra consumption TDO must be connected. An external pull-up resistor in the range of 47–100 kOhms should be added between the TDO pin and VDD. Only if the TDO pin is used as an application pin and a pull-up cannot be used should a pull-down resistor with the same value be used instead between the TDO pin and GND.

3.4 Voltage supply pins

Voltage supply pins are used to provide power to the device. Three dedicated pins are used for 1.2 V regulator stabilization.

Table 3. Voltage supply pin descriptions

Port pin	Function	Pin number		
		100 LQFP	144 LQFP	176 LQFP
VDD_HV	Digital supply voltage	15, 37, 52,70, 84	19, 51, 74,100,123	6, 27, 59, 90, 124,151
VSS	Digital ground	14, 18, 33,35,51,69,83,86	18, 22,47, 49,73,99,122,125	7, 26,30, 55,57,89,123,150,153
VDD_LV	1.2 V decoupling pins. Decoupling capacitor must be connected between these pins and the nearest V _{SS_LV} pin. ¹	19, 32, 85	23, 46, 124	31, 54, 98,152
VDD_BV	Internal regulator supply voltage	20	24	32
ADC_VRL	Reference ground and analog ground for the A/D converter	51	73	89
ADC_VRH	Reference voltage and analog supply for the A/D converter	52	74	90

3.5 Pad types

In the device the following types of pads are available for system pins and functional port pins:

S = Slow¹

M = Medium^{1 2}

F = Fast^{1 2}

I = Input only with analog feature¹

J = Input/Output ('S' pad) with analog feature

X = Oscillator

3.6 System pins

The system pins are listed in [Table 4](#).

Table 4. System pin descriptions

Port pin	Function	I/O direction	Pad type	RESET config.	Pin number		
					100 LQFP	144 LQFP	176 LQFP
RESET	Bidirectional reset with Schmitt-Trigger characteristics and noise filter.	I/O	M	Input weak pull-up after RGM PHASE2 and 40 FIRC cycles	17	21	29
EXTAL	Analog output of the oscillator amplifier circuit, when the oscillator is not in bypass mode. Analog input for the clock generator when the oscillator is in bypass mode.	I/O	X	Tristate	36	50	58
XTAL	Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator bypass mode is used.	I	X	Tristate	34	48	56

3.7 Functional port pins

The functional port pins are listed in [Table 5](#).

Table 5. Functional port pin descriptions

Port pin	PCR register	Alternative function ¹	Function	Peripheral	I/O	Pad type	RESET	Pin number				
								100 LQFP	144 LQFP	176 LQFP		
Port A												
PA[0]	PCR[0]	AF0 AF1 AF2 AF3 —	GPIO[0] E0UC[0] CLKOUT E0UC[13] WKPU[19] ⁵	SIUL eMIOS_0 MC_CGM eMIOS_0 WKPU	I/O I/O O I/O I	M	Tristate	12	16	24		
PA[1]	PCR[1]	AF0 AF1 AF2 AF3 —	GPIO[1] E0UC[1] NMI ⁶ CS1_6 WKPU[2] ⁵	SIUL eMIOS_0 WKPU DSPI_6 WKPU	I/O I/O I O I	S	Tristate	7	11	19		
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 — —	GPIO[2] E0UC[2] CS2_6 MA[2] WKPU[3] ⁵ LIN9RX	SIUL eMIOS_0 DSPI_6 ADC_0 WKPU LINFlex_9	I/O I/O O O I I	S	Tristate	5	9	17		

Table 4-3. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET config. ³	Pin number ⁴				
								100 LQFP	144 LQFP	176 LQFP		
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 — —	GPIO[3] E0UC[3] LIN5TX CS4_1 EIRQ[0] ADC1_S[0]	SIUL eMIOS_0 LINFlex_5 DSPI_1 SIUL ADC_1	I/O I/O O O I I	J	Tristate	68	90	114		
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 — —	GPIO[4] E0UC[4] — CS0_1 LIN5RX WKPU[9] ⁵	SIUL eMIOS_0 — DSPI_1 LINFlex_5 WKPU	I/O I/O — I/O I I	S	Tristate	29	43	51		
PA[5]	PCR[5]	AF0 AF1 AF2 AF3	GPIO[5] E0UC[5] LIN4TX CS3_6	SIUL eMIOS_0 LINFlex_4 DSPI_6	I/O I/O O O	M	Tristate	79	118	146		
PA[6]	PCR[6]	AF0 AF1 AF2 AF3 — —	GPIO[6] E0UC[6] — CS1_1 EIRQ[1] LIN4RX	SIUL eMIOS_0 — DSPI_1 SIUL LINFlex_4	I/O I/O — O I I	S	Tristate	80	119	147		
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 — —	GPIO[7] E0UC[7] LIN3TX SOUT_6 EIRQ[2] ADC1_S[1]	SIUL eMIOS_0 LINFlex_3 DSPI_6 SIUL ADC_1	I/O I/O O O I I	J	Tristate	71	104	128		
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — N/A ⁷ —	GPIO[8] E0UC[8] E0UC[14] SCK_6 EIRQ[3] ABS[0] LIN3RX	SIUL eMIOS_0 eMIOS_0 DSPI_6 SIUL BAM LINFlex_3	I/O I/O I/O I/O I I I	S	Input, weak pull-up	72	105	129		
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 N/A ⁷	GPIO[9] E0UC[9] — CS2_1 FAB	SIUL eMIOS_0 — DSPI_1 BAM	I/O I/O — O I	S	Pull-down	73	106	130		
PA[10]	PCR[10]	AF0 AF1 AF2 AF3 —	GPIO[10] E0UC[10] SDA_0 LIN2TX ADC1_S[2]	SIUL eMIOS_0 I2C_0 LINFlex_2 ADC_1	I/O I/O I/O O I	J	Tristate	74	107	131		

Port pin	PCR register	Alternative function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET config. ³	Pin number ⁴				
								100 LQFP	144 LQFP	176 LQFP		
PA[11]	PCR[11]	AF0 AF1 AF2 AF3 — — —	GPIO[11] E0UC[11] SCL_0 SOUT_7 EIRQ[16] LIN2RX ADC1_S[3]	SIUL Emios_0 I2C_0 DSPI_7 SIUL LINFlex_2 ADC_1	I/O I/O I/O O I I I	J	Tristate	75	108	132		
PA[12]	PCR[12]	AF0 AF1 AF2 AF3 — —	GPIO[12] — E0UC[28] CS3_1 EIRQ[17] SIN_0	SIUL — eMIOS_0 DSPI_1 SIUL DSPI_0	I/O — I/O O I I	S	Tristate	31	45	53		
PA[13]	PCR[13]	AF0 AF1 AF2 AF3	GPIO[13] SOUT_0 E0UC[29] —	SIUL DSPI_0 eMIOS_0 —	I/O O I/O —	M	Tristate	30	44	52		
PA[14]	PCR[14]	AF0 AF1 AF2 AF3 —	GPIO[14] SCK_0 CS0_0 E0UC[0] EIRQ[4]	SIUL DSPI_0 DSPI_0 eMIOS_0 SIUL	I/O I/O I/O I/O I	M	Tristate	28	42	50		
PA[15]	PCR[15]	AF0 AF1 AF2 AF3 —	GPIO[15] CS0_0 SCK_0 E0UC[1] WKPU[10] ⁵	SIUL DSPI_0 DSPI_0 eMIOS_0 WKPU	I/O I/O I/O I/O I	M	Tristate	27	40	48		
Port B												
PB[0]	PCR[16]	AF0 AF1 AF2 AF3	GPIO[16] CAN0TX E0UC[30] LIN0TX	SIUL FlexCAN_0 eMIOS_0 LINFlex_0	I/O O I/O O	M	Tristate	23	31	39		
PB[1]	PCR[17]	AF0 AF1 AF2 AF3 — — —	GPIO[17] — E0UC[31] SCK_7 WKPU[4] ⁵ CAN0RX LIN0RX	SIUL — eMIOS_0 DSPI_7 WKPU FlexCAN_0 LINFlex_0	I/O — I/O I/O I I I	S	Tristate	24	32	40		

Table 4-3. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET config. ³	Pin number ⁴				
								100 LQFP	144 LQFP	176 LQFP		
PB[2]	PCR[18]	AF0 AF1 AF2 AF3	GPIO[18] LIN0TX SDA_0 E0UC[30]	SIUL LINFlex_0 I2C_0 eMIOS_0	I/O O I/O I/O	M	Tristate	100	144	176		
PB[3]	PCR[19]	AF0 AF1 AF2 AF3 — —	GPIO[19] E0UC[31] SCL_0 CS0_6 WKPU[11] ⁵ LIN0RX	SIUL eMIOS_0 I2C_0 DSPI_6 WKPU LINFlex_0	I/O I/O I/O I/O I I	S	Tristate	1	1	1		
PB[4]	PCR[20]	AF0 AF1 AF2 AF3 — — —	— — — — ADC0_P[0] ADC1_P[0] GPIO[20]	— — — — ADC_0 ADC_1 SIUL	— — — — I I I	I	Tristate	50	72	88		
PB[5]	PCR[21]	AF0 AF1 AF2 AF3 — — —	— — — — ADC0_P[1] ADC1_P[1] GPIO[21]	— — — — ADC_0 ADC_1 SIUL	— — — — I I I	I	Tristate	53	75	91		
PB[6]	PCR[22]	AF0 AF1 AF2 AF3 — — —	— — — — ADC0_P[2] ADC1_P[2] GPIO[22]	— — — — ADC_0 ADC_1 SIUL	— — — — I I I	I	Tristate	54	76	92		
PB[7]	PCR[23]	AF0 AF1 AF2 AF3 — — — — —	— — — — ADC0_P[3] ADC1_P[3] GPIO[23] CAN7RX WKPU29	— — — — ADC_0 ADC_1 SIUL FlexCAN_7 WKPU	— — — — I I I I I	I	Tristate	55	77	93		

Port pin	PCR register	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET config. ³	Pin number ⁴				
								100 LQFP	144 LQFP	176 LQFP		
PB[8]	PCR[24]	AF0 AF1 AF2 AF3 — — — —	GPIO[24] — — — OSC32K_XTAL ⁸ WKPU[25] ⁵ ADC0_S[0] ADC1_S[4]	SIUL — — — OSC32K WKPU ADC_0 ADC_1	I — — — — I ⁹ I I	I	—	39	53	61		
PB[9]	PCR[25]	AF0 AF1 AF2 AF3 — — — —	GPIO[25] — — — OSC32K_EXTAL ⁸ WKPU[26] ⁵ ADC0_S[1] ADC1_S[5]	SIUL — — — OSC32K WKPU ADC_0 ADC_1	I — — — — I ⁹ I I	I	—	38	52	60		
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 — — — —	GPIO[26] — — CS1_7 WKPU[8] ⁵ ADC0_S[2] ADC1_S[6] CAN6RX	SIUL — — DSPI_7 WKPU ADC_0 ADC_1 FlexCAN_6	I/O — — O I I I I	J	Tristate	40	54	62		
PB[11]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] ETPUA[0] ¹³ CS0_0 ADC0_S[3]	SIUL eMIOS_0 ETPUA DSPI_0 ADC_0	I/O I/O I/O I/O I	J	Tristate	59	81	97		
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] ETPUA[1] ¹³ CS1_0 ADC0_X[0]	SIUL eMIOS_0 ETPUA DSPI_0 ADC_0	I/O I/O I/O O I	J	Tristate	61	83	101		
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] ETPUA[2] ¹³ CS2_0 ADC0_X[1]	SIUL eMIOS_0 ETPUA DSPI_0 ADC_0	I/O I/O I/O O I	J	Tristate	63	85	103		
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] ETPUA[3] ¹³ CS3_0 ADC0_X[2]	SIUL eMIOS_0 ETPUA DSPI_0 ADC_0	I/O I/O I/O O I	J	Tristate	65	87	105		

Table 4-3. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET config. ³	Pin number ⁴				
								100 LQFP	144 LQFP	176 LQFP		
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] ETPUA[4] ¹³ CS4_0 ADC0_X[3]	SIUL eMIOS_0 ETPUA DSPI_0 ADC_0	I/O I/O I/O O I	J	Tristate	67	89	107		
Port C												
PC[0] ¹⁰	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI CS2_7	SIUL — JTAGC DSPI_7	I/O — I O	M	Input, weak pull-up	87	126	154		
PC[1] ¹⁰	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO CS3_7	SIUL — JTAGC DSPI_7	I/O — O O	F ¹¹	Tristate	82	121	149		
PC[2]	PCR[34]	AF0 AF1 AF2 AF3 —	GPIO[34] SCK_1 CAN4TX DEBUG[0] EIRQ[5]	SIUL DSPI_1 FlexCAN_4 SSCM SIUL	I/O I/O O O I	M	Tristate	78	117	145		
PC[3]	PCR[35]	AF0 AF1 AF2 AF3 — — — —	GPIO[35] CS0_1 MA[0] DEBUG[1] EIRQ[6] CAN1RX CAN4RX WKPU30	SIUL DSPI_1 ADC_0 SSCM SIUL FlexCAN_1 FlexCAN_4 WKPU	I/O I/O O O I I I I	S	Tristate	77	116	144		
PC[4]	PCR[36]	AF0 AF1 AF2 AF3 — — — —	GPIO[36] E1UC[31] CS4_6 DEBUG[2] EIRQ[18] SIN_1 CAN3RX WKPU31	SIUL eMIOS_1 DSPI_6 SSCM SIUL DSPI_1 FlexCAN_3 WKPU	I/O I/O O O I I I I	M	Tristate	92	131	159		
PC[5]	PCR[37]	AF0 AF1 AF2 AF3 —	GPIO[37] SOUT_1 CAN3TX DEBUG[3] EIRQ[7]	SIUL DSPI_1 FlexCAN_3 SSCM SIUL	I/O O O O I	M	Tristate	91	130	158		

Port pin	PCR register	Alternative function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET config. ³	Pin number ⁴				
								100 LQFP	144 LQFP	176 LQFP		
PC[6]	PCR[38]	AF0 AF1 AF2 AF3 —	GPIO[38] LIN1TX E1UC[28] DEBUG[4] SIN_6	SIUL LINFlex_1 eMIOS_1 SSCM DSPI_6	I/O O I/O O I	S	Tristate	25	36	44		
PC[7]	PCR[39]	AF0 AF1 AF2 AF3 — —	GPIO[39] — E1UC[29] DEBUG[5] LIN1RX WKPU[12] ⁵	SIUL — eMIOS_1 SSCM LINFlex_1 WKPU	I/O — I/O O I I	S	Tristate	26	37	45		
PC[8]	PCR[40]	AF0 AF1 AF2 AF3 —	GPIO[40] LIN2TX E0UC[3] DEBUG[6] SIN_7	SIUL LINFlex_2 eMIOS_0 SSCM DSPI_7	I/O O I/O O I	S	Tristate	99	143	175		
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — E0UC[7] DEBUG[7] WKPU[13] ⁵ LIN2RX	SIUL — eMIOS_0 SSCM WKPU LINFlex_2	I/O — I/O O I I	S	Tristate	2	2	2		
PC[10]	PCR[42]	AF0 AF1 AF2 AF3 —	GPIO[42] CAN1TX CAN4TX MA[1] SIN_8	SIUL FlexCAN_1 FlexCAN_4 ADC_0 DSPI_8	I/O O O O I	M	Tristate	22	28	36		
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 — — —	GPIO[43] — SDA_1 MA[2] WKPU[5] ⁵ CAN1RX CAN4RX	SIUL — I2C_1 ADC_0 WKPU FlexCAN_1 FlexCAN_4	I/O — I/O O I I I	S	Tristate	21	27	35		
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 — —	GPIO[44] E0UC[12] SCL_1 ETPUA[5] ¹³ EIRQ[19] SIN_2	SIUL eMIOS_0 I2C_1 ETPUA SIUL DSPI_2	I/O I/O I/O I/O I I	M	Tristate	97	141	173		
PC[13]	PCR[45]	AF0 AF1 AF2 AF3	GPIO[45] E0UC[13] SOUT_2 ETPUA[6] ¹³	SIUL eMIOS_0 DSPI_2 ETPUA	I/O I/O O I/O	S	Tristate	98	142	174		

Table 4-3. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET config. ³	Pin number ⁴				
								100 LQFP	144 LQFP	176 LQFP		
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 —	GPIO[46] E0UC[14] SCK_2 ETPUA[7] ¹³ EIRQ[8]	SIUL eMIOS_0 DSPI_2 ETPUA SIUL	I/O I/O I/O I/O I	S	Tristate	3	3	3		
PC[15]	PCR[47]	AF0 AF1 AF2 AF3 —	GPIO[47] E0UC[15] CS0_2 ETPUA[8] ¹³ EIRQ[20]	SIUL eMIOS_0 DSPI_2 ETPUA SIUL	I/O I/O I/O I/O I	M	Tristate	4	4	4		
Port D												
PD[0]	PCR[48]	AF0 AF1 AF2 AF3 — — —	GPIO[48] — — — WKPU[27] ⁵ ADC0_P[4] ADC1_P[4]	SIUL — — — WKPU ADC_0 ADC_1	I — — — I I I	I	Tristate	41	63	77		
PD[1]	PCR[49]	AF0 AF1 AF2 AF3 — — —	GPIO[49] — — — WKPU[28] ⁵ ADC0_P[5] ADC1_P[5]	SIUL — — — WKPU ADC_0 ADC_1	I — — — I I I	I	Tristate	42	64	78		
PD[2]	PCR[50]	AF0 AF1 AF2 AF3 — —	GPIO[50] — — — ADC0_P[6] ADC1_P[6]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	43	65	79		
PD[3]	PCR[51]	AF0 AF1 AF2 AF3 — —	GPIO[51] — — — ADC0_P[7] ADC1_P[7]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	44	66	80		
PD[4]	PCR[52]	AF0 AF1 AF2 AF3 — —	GPIO[52] — — — ADC0_P[8] ADC1_P[8]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	45	67	81		

Port pin	PCR register	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET config. ³	Pin number ⁴				
								100 LQFP	144 LQFP	176 LQFP		
PD[5]	PCR[53]	AF0 AF1 AF2 AF3 — —	GPIO[53] — — — ADC0_P[9] ADC1_P[9]	SIUL — — — ADC_0 ADC_1	 — — — 		Tristate	46	68	82		
PD[6]	PCR[54]	AF0 AF1 AF2 AF3 — —	GPIO[54] — — — ADC0_P[10] ADC1_P[10]	SIUL — — — ADC_0 ADC_1	 — — — 		Tristate	47	69	83		
PD[7]	PCR[55]	AF0 AF1 AF2 AF3 — —	GPIO[55] — — — ADC0_P[11] ADC1_P[11]	SIUL — — — ADC_0 ADC_1	 — — — 		Tristate	48	70	84		
PD[8]	PCR[56]	AF0 AF1 AF2 AF3 — —	GPIO[56] — — — ADC0_P[12] ADC1_P[12]	SIUL — — — ADC_0 ADC_1	 — — — 		Tristate	49	71	87		
PD[9]	PCR[57]	AF0 AF1 AF2 AF3 — —	GPIO[57] — — — ADC0_P[13] ADC1_P[13]	SIUL — — — ADC_0 ADC_1	 — — — 		Tristate	56	78	94		
PD[10]	PCR[58]	AF0 AF1 AF2 AF3 — —	GPIO[58] — TCK_A — ADC0_P[14] ADC1_P[14]	SIUL — ETPUA — ADC_0 ADC_1	 — — 		Tristate	57	79	95		
PD[11]	PCR[59]	AF0 AF1 AF2 AF3 — —	GPIO[59] — TCK_B — ADC0_P[15] ADC1_P[15]	SIUL — ETPUB — ADC_0 ADC_1	 — — 		Tristate	58	80	96		

Table 4-3. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET config. ³	Pin number ⁴				
								100 LQFP	144 LQFP	176 LQFP		
PD[12]	PCR[60]	AF0 AF1 AF2 AF3 —	GPIO[60] CS5_0 E0UC[24] ETPUA[9] ¹³ ADC0_S[4]	SIUL DSPI_0 eMIOS_0 ETPUA ADC_0	I/O O I/O I/O I	J	Tristate	60	82	100		
PD[13]	PCR[61]	AF0 AF1 AF2 AF3 —	GPIO[61] CS0_1 E0UC[25] ETPUA[10] ¹³ ADC0_S[5]	SIUL DSPI_1 eMIOS_0 ETPUA ADC_0	I/O I/O I/O I/O I	J	Tristate	62	84	102		
PD[14]	PCR[62]	AF0 AF1 AF2 AF3 —	GPIO[62] CS1_1 E0UC[26] ETPUA[11] ¹³ ADC0_S[6]	SIUL DSPI_1 eMIOS_0 ETPUA ADC_0	I/O O I/O I/O I	J	Tristate	64	86	104		
PD[15]	PCR[63]	AF0 AF1 AF2 AF3 —	GPIO[63] CS2_1 E0UC[27] ETPUA[12] ¹³ ADC0_S[7]	SIUL DSPI_1 eMIOS_0 ETPUA ADC_0	I/O O I/O I/O I	J	Tristate	66	88	106		
Port E												
PE[0]	PCR[64]	AF0 AF1 AF2 AF3 — —	GPIO[64] E0UC[16] LIN10TX ETPUA[13] ¹³ WKPU[6] ⁵ CAN5RX	SIUL eMIOS_0 LINFlex_10 ETPUA WKPU FlexCAN_5	I/O I/O O I/O I I	S	Tristate	6	10	18		
PE[1]	PCR[65]	AF0 AF1 AF2 AF3 —	GPIO[65] E0UC[17] CAN5TX ETPUA[14] ¹³ LIN10RX	SIUL eMIOS_0 FlexCAN_5 ETPUA LINFlex_10	I/O I/O O I/O I	M	Tristate	8	12	20		
PE[2]	PCR[66]	AF0 AF1 AF2 AF3 — —	GPIO[66] E0UC[18] CAN6TX ETPUA[15] ¹³ EIRQ[21] SIN_1	SIUL eMIOS_0 FlexCAN_6 ETPUA SIUL DSPI_1	I/O I/O O I/O I I	M	Tristate	89	128	156		
PE[3]	PCR[67]	AF0 AF1 AF2 AF3	GPIO[67] E0UC[19] SOUT_1 ETPUA[16] ¹³	SIUL eMIOS_0 DSPI_1 ETPUA	I/O I/O O I/O	M	Tristate	90	129	157		

Port pin	PCR register	Alternative function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET config. ³	Pin number ⁴				
								100 LQFP	144 LQFP	176 LQFP		
PE[4]	PCR[68]	AF0 AF1 AF2 AF3 —	GPIO[68] E0UC[20] SCK_1 ETPUA[17] ¹³ EIRQ[9]	SIUL eMIOS_0 DSPI_1 ETPUA SIUL	I/O I/O I/O I/O I	M	Tristate	93	132	160		
PE[5]	PCR[69]	AF0 AF1 AF2 AF3	GPIO[69] E0UC[21] CS0_1 MA[2]	SIUL eMIOS_0 DSPI_1 ADC_0	I/O I/O I/O O	M	Tristate	94	133	161		
PE[6]	PCR[70]	AF0 AF1 AF2 AF3 —	GPIO[70] E0UC[22] CS3_0 MA[1] EIRQ[22]	SIUL eMIOS_0 DSPI_0 ADC_0 SIUL	I/O I/O O O I	M	Tristate	95	139	167		
PE[7]	PCR[71]	AF0 AF1 AF2 AF3 —	GPIO[71] E0UC[23] CS2_0 MA[0] EIRQ[23]	SIUL eMIOS_0 DSPI_0 ADC_0 SIUL	I/O I/O O O I	M	Tristate	96	140	168		
PE[8]	PCR[72]	AF0 AF1 AF2 AF3	GPIO[72] CAN2TX E0UC[22] CAN3TX	SIUL FlexCAN_2 eMIOS_0 FlexCAN_3	I/O O I/O O	M	Tristate	9	13	21		
PE[9]	PCR[73]	AF0 AF1 AF2 AF3 — — —	GPIO[73] CS4_7 E0UC[23] ETPUA[18] ¹³ WKPU[7] ⁵ CAN2RX CAN3RX	SIUL DSPI_7 eMIOS_0 ETPUA WKPU FlexCAN_2 FlexCAN_3	I/O O I/O I/O I I I	S	Tristate	10	14	22		
PE[10]	PCR[74]	AF0 AF1 AF2 AF3 —	GPIO[74] LIN3TX CS3_1 E1UC[30] EIRQ[10]	SIUL LINFlex_3 DSPI_1 eMIOS_1 SIUL	I/O O O I/O I	S	Tristate	11	15	23		
PE[11]	PCR[75]	AF0 AF1 AF2 AF3 — —	GPIO[75] E0UC[24] CS4_1 ETPUA[19] ¹³ LIN3RX WKPU[14] ⁵	SIUL eMIOS_0 DSPI_1 ETPUA LINFlex_3 WKPU	I/O I/O O I/O I I	S	Tristate	13	17	25		

Table 4-3. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET config. ³	Pin number ⁴				
								100 LQFP	144 LQFP	176 LQFP		
PE[12]	PCR[76]	AF0 AF1 AF2 AF3 — — —	GPIO[76] CAN7TX E1UC[19] ¹² ETPUA[20] ¹³ EIRQ[11] SIN_2 ADC1_S[7]	SIUL FlexCAN_7 eMIOS_1 ETPUA SIUL DSPI_2 ADC_1	I/O O I/O I/O I I I	J	Tristate	76	109	133		
PE[13]	PCR[77]	AF0 AF1 AF2 AF3	GPIO[77] SOUT_2 E1UC[20] ETPUA[21] ¹³	SIUL DSPI_2 eMIOS_1 ETPUA	I/O O I/O I/O	S	Tristate	—	103	127		
PE[14]	PCR[78]	AF0 AF1 AF2 AF3 —	GPIO[78] SCK_2 E1UC[21] ETPUA[22] ¹³ EIRQ[12]	SIUL DSPI_2 eMIOS_1 ETPUA SIUL	I/O I/O I/O I/O I	S	Tristate	—	112	136		
PE[15]	PCR[79]	AF0 AF1 AF2 AF3	GPIO[79] CS0_2 E1UC[22] ETPUA[23] ¹³	SIUL DSPI_2 eMIOS_1 ETPUA	I/O I/O I/O I/O	M	Tristate	—	113	137		
Port F												
PF[0]	PCR[80]	AF0 AF1 AF2 AF3 —	GPIO[80] E0UC[10] CS3_1 ETPUA[24] ¹³ ADC0_S[8]	SIUL eMIOS_0 DSPI_1 ETPUA ADC_0	I/O I/O O I/O I	J	Tristate	—	55	63		
PF[1]	PCR[81]	AF0 AF1 AF2 AF3 —	GPIO[81] E0UC[11] CS4_1 ETPUA[25] ¹³ ADC0_S[9]	SIUL eMIOS_0 DSPI_1 ETPUA ADC_0	I/O I/O O I/O I	J	Tristate	—	56	64		
PF[2]	PCR[82]	AF0 AF1 AF2 AF3 —	GPIO[82] E0UC[12] CS0_2 ETPUA[26] ¹³ ADC0_S[10]	SIUL eMIOS_0 DSPI_2 ETPUA ADC_0	I/O I/O I/O I/O I	J	Tristate	—	57	65		
PF[3]	PCR[83]	AF0 AF1 AF2 AF3 —	GPIO[83] E0UC[13] CS1_2 ETPUA[27] ¹³ ADC0_S[11]	SIUL eMIOS_0 DSPI_2 ETPUA ADC_0	I/O I/O O I/O I	J	Tristate	—	58	66		

Port pin	PCR register	Alternative function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET config. ³	Pin number ⁴				
								100 LQFP	144 LQFP	176 LQFP		
PF[4]	PCR[84]	AF0 AF1 AF2 AF3 —	GPIO[84] E0UC[14] CS2_2 ETPUA[28] ¹³ ADC0_S[12]	SIUL eMIOS_0 DSPI_2 ETPUA ADC_0	I/O I/O O I/O I	J	Tristate	—	59	67		
PF[5]	PCR[85]	AF0 AF1 AF2 AF3 —	GPIO[85] E0UC[22] CS3_2 ETPUA[29] ¹³ ADC0_S[13]	SIUL eMIOS_0 DSPI_2 ETPUA ADC_0	I/O I/O O I/O I	J	Tristate	—	60	68		
PF[6]	PCR[86]	AF0 AF1 AF2 AF3 —	GPIO[86] E0UC[23] CS1_1 ETPUA[30] ¹³ ADC0_S[14]	SIUL eMIOS_0 DSPI_1 ETPUA ADC_0	I/O I/O O I/O I	J	Tristate	—	61	69		
PF[7]	PCR[87]	AF0 AF1 AF2 AF3 —	GPIO[87] — CS2_1 ETPUA[31] ¹³ ADC0_S[15]	SIUL — DSPI_1 ETPUA ADC_0	I/O — O I/O I	J	Tristate	—	62	70		
PF[8]	PCR[88]	AF0 AF1 AF2 AF3	GPIO[88] CAN3TX CS4_0 CAN2TX	SIUL FlexCAN_3 DSPI_0 FlexCAN_2	I/O O O O	M	Tristate	—	34	42		
PF[9]	PCR[89]	AF0 AF1 AF2 AF3 — — —	GPIO[89] E1UC[1] CS5_0 — WKPU[22] ⁵ CAN2RX CAN3RX	SIUL eMIOS_1 DSPI_0 — WKPU FlexCAN_2 FlexCAN_3	I/O I/O O — I I I	S	Tristate	—	33	41		
PF[10]	PCR[90]	AF0 AF1 AF2 AF3	GPIO[90] CS1_0 LIN4TX E1UC[2]	SIUL DSPI_0 LINFlex_4 eMIOS_1	I/O O O I/O	M	Tristate	—	38	46		
PF[11]	PCR[91]	AF0 AF1 AF2 AF3 — —	GPIO[91] CS2_0 E1UC[3] ETPUB[0] ¹³ WKPU[15] ⁵ LIN4RX	SIUL DSPI_0 eMIOS_1 ETPUB WKPU LINFlex_4	I/O O I/O I/O I I	S	Tristate	—	39	47		

Table 4-3. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET config. ³	Pin number ⁴				
								100 LQFP	144 LQFP	176 LQFP		
PF[12]	PCR[92]	AF0 AF1 AF2 AF3	GPIO[92] E1UC[25] LIN5TX ETPUB[1] ¹³	SIUL eMIOS_1 LINFlex_5 ETPUB	I/O I/O O I/O	M	Tristate	—	35	43		
PF[13]	PCR[93]	AF0 AF1 AF2 AF3 — —	GPIO[93] E1UC[26] CS5_7 ETPUB[2] ¹³ WKPU[16] ⁵ LIN5RX	SIUL eMIOS_1 DSPI_7 ETPUB WKPU LINFlex_5	I/O I/O O I/O I I	S	Tristate	—	41	49		
PF[14]	PCR[94]	AF0 AF1 AF2 AF3	GPIO[94] CAN4TX E1UC[27] CAN1TX	SIUL FlexCAN_4 eMIOS_1 FlexCAN_1	I/O O I/O O	M	Tristate	—	102	126		
PF[15]	PCR[95]	AF0 AF1 AF2 AF3 — — —	GPIO[95] E1UC[4] — ETPUB[3] ¹³ EIRQ[13] CAN1RX CAN4RX	SIUL eMIOS_1 — ETPUB SIUL FlexCAN_1 FlexCAN_4	I/O I/O — I/O I I I	S	Tristate	—	101	125		
Port G												
PG[0]	PCR[96]	AF0 AF1 AF2 AF3	GPIO[96] CAN5TX E1UC[23] ETPUB[4] ¹³	SIUL FlexCAN_5 eMIOS_1 ETPUB	I/O O I/O I/O	M	Tristate	—	98	122		
PG[1]	PCR[97]	AF0 AF1 AF2 AF3 — —	GPIO[97] — E1UC[24] ETPUB[5] ¹³ EIRQ[14] CAN5RX	SIUL — eMIOS_1 ETPUB SIUL FlexCAN_5	I/O — I/O I/O I I	S	Tristate	—	97	121		
PG[2]	PCR[98]	AF0 AF1 AF2 AF3	GPIO[98] E1UC[11] SOUT_3 ETPUB[6] ¹³	SIUL eMIOS_1 DSPI_3 ETPUB	I/O I/O O I/O	M	Tristate	—	8	16		

Port pin	PCR register	Alternative function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET config. ³	Pin number ⁴				
								100 LQFP	144 LQFP	176 LQFP		
PG[3]	PCR[99]	AF0 AF1 AF2 AF3 —	GPIO[99] E1UC[12] CS0_3 ETPUB[7] ¹³ WKPU[17] ⁵	SIUL eMIOS_1 DSPI_3 ETPUB WKPU	I/O I/O I/O I/O I	S	Tristate	—	7	15		
PG[4]	PCR[100]	AF0 AF1 AF2 AF3	GPIO[100] E1UC[13] SCK_3 ETPUB[8] ¹³	SIUL eMIOS_1 DSPI_3 ETPUB	I/O I/O I/O —	M	Tristate	—	6	14		
PG[5]	PCR[101]	AF0 AF1 AF2 AF3 — —	GPIO[101] E1UC[14] CS1_8 ETPUB[9] ¹³ WKPU[18] ⁵ SIN_3	SIUL eMIOS_1 DSPI_8 ETPUB WKPU DSPI_3	I/O I/O O I/O I I	S	Tristate	—	5	13		
PG[6]	PCR[102]	AF0 AF1 AF2 AF3	GPIO[102] E1UC[15] LIN6TX ETPUB[10] ¹³	SIUL eMIOS_1 LINFlex_6 ETPUB	I/O I/O O I/O	M	Tristate	—	30	38		
PG[7]	PCR[103]	AF0 AF1 AF2 AF3 — —	GPIO[103] E1UC[16] E1UC[30] ETPUB[11] ¹³ WKPU[20] ⁵ LIN6RX	SIUL eMIOS_1 eMIOS_1 ETPUB WKPU LINFlex_6	I/O I/O I/O I/O I I	S	Tristate	—	29	37		
PG[8]	PCR[104]	AF0 AF1 AF2 AF3 —	GPIO[104] E1UC[17] LIN7TX CS0_2 EIRQ[15]	SIUL eMIOS_1 LINFlex_7 DSPI_2 SIUL	I/O I/O O I/O I	S	Tristate	—	26	34		
PG[9]	PCR[105]	AF0 AF1 AF2 AF3 — —	GPIO[105] E1UC[18] — SCK_2 WKPU[21] ⁵ LIN7RX	SIUL eMIOS_1 — DSPI_2 WKPU LINFlex_7	I/O I/O — I/O I I	S	Tristate	—	25	33		
PG[10]	PCR[106]	AF0 AF1 AF2 AF3 —	GPIO[106] E0UC[24] E1UC[31] ETPUB[12] ¹³ SIN_4	SIUL eMIOS_0 eMIOS_1 ETPUB DSPI_4	I/O I/O I/O I/O I	S	Tristate	—	114	138		

Table 4-3. Functional port pin descriptions (continued)

Port pin	PCR register	Alternative function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET config. ³	Pin number ⁴				
								100 LQFP	144 LQFP	176 LQFP		
PG[11]	PCR[107]	AF0 AF1 AF2 AF3	GPIO[107] E0UC[25] CS0_4 ETPUB[13] ¹³	SIUL eMIOS_0 DSPI_4 ETPUB	I/O I/O I/O I/O	M	Tristate	—	115	139		
PG[12]	PCR[108]	AF0 AF1 AF2 AF3	GPIO[108] E0UC[26] SOUT_4 ETPUB[14] ¹³	SIUL eMIOS_0 DSPI_4 ETPUB	I/O I/O O I/O	M	Tristate	—	92	116		
PG[13]	PCR[109]	AF0 AF1 AF2 AF3	GPIO[109] E0UC[27] SCK_4 ETPUB[15] ¹³	SIUL eMIOS_0 DSPI_4 ETPUB	I/O I/O I/O I/O	M	Tristate	—	91	115		
PG[14]	PCR[110]	AF0 AF1 AF2 AF3	GPIO[110] E1UC[0] LIN8TX ETPUB[16] ¹³	SIUL eMIOS_1 LINFlex_8 ETPUB	I/O I/O O I/O	S	Tristate	—	110	134		
PG[15]	PCR[111]	AF0 AF1 AF2 AF3 —	GPIO[111] E1UC[1] CS2_8 ETPUB[17] ¹³ LIN8RX	SIUL eMIOS_1 DSPI_8 ETPUB LINFlex_8	I/O I/O O I/O I	M	Tristate	—	111	135		
Port H												
PH[0]	PCR[112]	AF0 AF1 AF2 AF3 —	GPIO[112] E1UC[2] LIN13TX ETPUB[18] ¹³ SIN_1	SIUL eMIOS_1 LIN_Flex13 ETPUB DSPI_1	I/O I/O O I/O I	M	Tristate	—	93	117		
PH[1]	PCR[113]	AF0 AF1 AF2 AF3 —	GPIO[113] E1UC[3] SOUT_1 ETPUB[19] ¹³ LIN13RX	SIUL eMIOS_1 DSPI_1 ETPUB LINFlex_13	I/O I/O O I/O I	M	Tristate	—	94	118		
PH[2]	PCR[114]	AF0 AF1 AF2 AF3	GPIO[114] E1UC[4] SCK_1 ETPUB[20] ¹³	SIUL eMIOS_1 DSPI_1 ETPUB	I/O I/O I/O I/O	M	Tristate	—	95	119		
PH[3]	PCR[115]	AF0 AF1 AF2 AF3	GPIO[115] E1UC[5] CS0_1 ETPUB[21] ¹³	SIUL eMIOS_1 DSPI_1 ETPUB	I/O I/O I/O I/O	M	Tristate	—	96	120		
PH[4]	PCR[116]	AF0 AF1 AF2 AF3	GPIO[116] E1UC[6] LIN11TX ETPUB[22] ¹³	SIUL eMIOS_1 LIN_Flex11 ETPUB	I/O I/O O I/O	M	Tristate	—	134	162		

Port pin	PCR register	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET config. ³	Pin number ⁴				
								100 LQFP	144 LQFP	176 LQFP		
PH[5]	PCR[117]	AF0 AF1 AF2 AF3 —	GPIO[117] E1UC[7] — ETPUB[23] ¹³ LIN11RX	SIUL eMIOS_1 — ETPUB LINFlex_11	I/O I/O — I/O	S	Tristate	—	135	163		
PH[6]	PCR[118]	AF0 AF1 AF2 AF3	GPIO[118] E1UC[8] CS3_8 MA[2]	SIUL eMIOS_1 DSPI_8 ADC_0	I/O I/O O O	M	Tristate	—	136	164		
PH[7]	PCR[119]	AF0 AF1 AF2 AF3	GPIO[119] E1UC[9] CS3_2 MA[1]	SIUL eMIOS_1 DSPI_2 ADC_0	I/O I/O O O	M	Tristate	—	137	165		
PH[8]	PCR[120]	AF0 AF1 AF2 AF3	GPIO[120] E1UC[10] CS2_2 MA[0]	SIUL eMIOS_1 DSPI_2 ADC_0	I/O I/O O O	M	Tristate	—	138	166		
PH[9] ¹⁰	PCR[121]	AF0 AF1 AF2 AF3	GPIO[121] CS0_7 TCK SDA_1	SIUL DSPI_7 JTAGC I2C_1	I/O I/O I I/O	S	Input, weak pull-up	88	127	155		
PH[10] ¹⁰	PCR[122]	AF0 AF1 AF2 AF3	GPIO[122] — TMS SCL_1	SIUL — JTAGC I2C_1	I/O — I I/O	M	Input, weak pull-up	81	120	148		
PH[11]	PCR[123]	AF0 AF1 AF2 AF3	GPIO[123] SOUT_3 CS0_4 E1UC[5]	SIUL DSPI_3 DSPI_4 eMIOS_1	I/O O I/O I/O	M	Tristate	—	—	140		
PH[12]	PCR[124]	AF0 AF1 AF2 AF3	GPIO[124] SCK_3 CS1_4 E1UC[25]	SIUL DSPI_3 DSPI_4 eMIOS_1	I/O I/O O I/O	M	Tristate	—	—	141		
PH[13]	PCR[125]	AF0 AF1 AF2 AF3	GPIO[125] SOUT_4 CS0_3 E1UC[26]	SIUL DSPI_4 DSPI_3 eMIOS_1	I/O O I/O I/O	M	Tristate	—	—	9		
PH[14]	PCR[126]	AF0 AF1 AF2 AF3	GPIO[126] SCK_4 CS1_3 E1UC[27]	SIUL DSPI_4 DSPI_3 eMIOS_1	I/O I/O O I/O	M	Tristate	—	—	10		

Table 4-3. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET config. ³	Pin number ⁴				
								100 LQFP	144 LQFP	176 LQFP		
PH[15]	PCR[127]	AF0 AF1 AF2 AF3	GPIO[127] SOUT_5 CS0_8 E1UC[17]	SIUL DSPI_5 DSPI_8 eMIOS_1	I/O O I/O I/O	M	Tristate	—	—	8		
Port I												
PI[0]	PCR[128]	AF0 AF1 AF2 AF3	GPIO[128] E0UC[28] LIN8TX SOUT_8(lvdsp)	SIUL eMIOS_0 LINFlex_8 DSPI_8	I/O I/O O O	S	Tristate	—	—	172		
PI[1]	PCR[129]	AF0 AF1 AF2 AF3 — —	GPIO[129] E0UC[29] LIN12TX SOUT_8(lvdsm) WKPU[24] ⁵ LIN8RX	SIUL eMIOS_0 LINFlex_12 DSPI_8 WKPU LINFlex_8	I/O I/O O O I I	S	Tristate	—	—	171		
PI[2]	PCR[130]	AF0 AF1 AF2 AF3	GPIO[130] E0UC[30] LIN9TX SCK_8(lvdsp)	SIUL eMIOS_0 LINFlex_9 DSPI_8	I/O I/O O I/O	S	Tristate	—	—	170		
PI[3]	PCR[131]	AF0 AF1 AF2 AF3 — —	GPIO[131] E0UC[31] — SCK_8(lvdsm) WKPU[23] ⁵ LIN9RX	SIUL eMIOS_0 — DSPI_8 WKPU LINFlex_9	I/O I/O — I/O I I	S	Tristate	—	—	169		
PI[4]	PCR[132]	AF0 AF1 AF2 AF3	GPIO[132] E1UC[28] SOUT_4 ETPUB[24] ¹³	SIUL eMIOS_1 DSPI_4 ETPUB	I/O I/O O I/O	S	Tristate	—	—	143		
PI[5]	PCR[133]	AF0 AF1 AF2 AF3	GPIO[133] E1UC[29] SCK_4 ETPUB[25] ¹³	SIUL eMIOS_1 DSPI_4 ETPUB	I/O I/O I/O I/O	S	Tristate	—	—	142		
PI[6]	PCR[134]	AF0 AF1 AF2 AF3	GPIO[134] E1UC[30] CS0_4 ETPUB[26] ¹³	SIUL eMIOS_1 DSPI_4 ETPUB	I/O I/O I/O I/O	S	Tristate	—	—	11		
PI[7]	PCR[135]	AF0 AF1 AF2 AF3	GPIO[135] E1UC[31] CS1_4 ETPUB[27] ¹³	SIUL eMIOS_1 DSPI_4 ETPUB	I/O I/O O I/O	S	Tristate	—	—	12		

Port pin	PCR register	Alternative function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET config. ³	Pin number ⁴				
								100 LQFP	144 LQFP	176 LQFP		
PI[8]	PCR[136]	AF0 AF1 AF2 AF3 —	GPIO[136] CAN6TX SOUT_8 ETPUB[28] ¹³ ADC0_S[16]	SIUL FLEXCAN_6 DSPI_8 ETPUB ADC_0	I/O O O I/O I	J	Tristate	—	—	108		
PI[9]	PCR[137]	AF0 AF1 AF2 AF3 —	GPIO[137] CAN7TX SCK_8 ETPUB[29] ¹³ — ADC0_S[17]	SIUL FLEXCAN_7 DSPI_8 ETPUB — ADC_0	I/O O I/O I/O — I	J	Tristate	—	—	109		
PI[10]	PCR[138]	AF0 AF1 AF2 AF3 —	GPIO[138] CAN6RX CS4_8 ETPUB[30] ¹³ ADC0_S[18]	SIUL FLEXCAN_6 DSPI_8 ETPUB ADC_0	I/O I O I/O I	J	Tristate	—	—	110		
PI[11]	PCR[139]	AF0 AF1 AF2 AF3 — —	GPIO[139] CAN7RX CS5_8 ETPUB[31] ¹³ — ADC0_S[19] SIN_3	SIUL FLEXCAN_7 DSPI_8 ETPUB ¹³ — ADC_0 DSPI_3	I/O I I/O — I I	J	Tristate	—	—	111		
PI[12]	PCR[140]	AF0 AF1 AF2 AF3 —	GPIO[140] CS0_3 SDA_2 LIN11TX ADC0_S[20]	SIUL DSPI_3 I2C_2 LINFlex_11 ADC_0	I/O I/O I/O O I	J	Tristate	—	—	112		
PI[13]	PCR[141]	AF0 AF1 AF2 AF3 —	GPIO[141] CS1_3 SCL_2 LIN10TX ADC0_S[21]	SIUL DSPI_3 I2C_2 LINFlex_10 ADC_0	I/O O I/O O I	J	Tristate	—	—	113		

Table 4-3. Functional port pin descriptions (continued)

PI[14]	PCR[142]]	AF0 AF1 AF2 AF3 — —	GPIO[142] — SDA_3 — ADC0_S[22] SIN_4	SIUL — I2C_3 — ADC_0 DSPI_4	I/O — I/O — I I	J	Tristate	—	—	76		
PI[15]	PCR[143]]	AF0 AF1 AF2 AF3 —	GPIO[143] CS0_4 SCL_3 LIN9TX ADC0_S[23]	SIUL DSPI_4 I2C_3 LINFlex_9 ADC_0	I/O I/O I/O O I	J	Tristate	—	—	75		
Port J												

Port pin	PCR register	Alternative function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET config. ³	Pin number ⁴				
								100 LQFP	144 LQFP	176 LQFP		
PJ[0]	PCR[144]	AF0 AF1 AF2 AF3 — —	GPIO[144] CS1_4 — SDA_2 ADC0_S[24] LIN12RX	SIUL DSPI_4 — I2C_2 ADC_0 LINFlex_12	I/O O — I/O I I	J	Tristate	—	—	74		
PJ[1]	PCR[145]	AF0 AF1 AF2 AF3 — —	GPIO[145] — LIN13TX CS5_6 ADC0_S[25] SIN_5	SIUL — LINFlex_13 DSPI_6 ADC_0 DSPI_5	I/O — O O I I	J	Tristate	—	—	73		
PJ[2]	PCR[146]	AF0 AF1 AF2 AF3 —	GPIO[146] CS0_5 SDA_3 SCL_2 ADC0_S[26]	SIUL DSPI_5 I2C_3 I2C_2 ADC_0	I/O I/O I/O I/O I	J	Tristate	—	—	72		
PJ[3]	PCR[147]	AF0 AF1 AF2 AF3 —	GPIO[147] CS1_5 LIN12TX — ADC0_S[27]	SIUL DSPI_5 LINFlex_12 — ADC_0	I/O O O — I	J	Tristate	—	—	71		
PJ[4]	PCR[148]	AF0 AF1 AF2 AF3	GPIO[148] SCK_5 E1UC[18] SCL_3	SIUL DSPI_5 eMIOS_1 I2C_3	I/O I/O I/O I/O	M	Tristate	—	—	5		
PJ[5]	PCR[149]	—	MDO0	NDI	O	F	Tristate	—	—	—		
PJ[6]	PCR[150]	—	MDO1	NDI	O	F	Tristate	—	—	—		
PJ[7]	PCR[151]	—	MDO2	NDI	O	F	Tristate	—	—	—		
PJ[8]	PCR[152]	—	MDO3	NDI	O	F	Tristate	—	—	—		
PJ[9]	PCR[153]	AF0	MSEO	NDI	O	F	Output	—	—	—		

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PJ[10]	PCR[154]]	AF0	MCKO	NDI	O	F	Output	—	—	—		
PJ[11]	PCR[155]]	AF0	EVTI	NDI	I	F	Input, weak pull-up	—	—	—		
PJ[12]	PCR[156]]	AF0	EVTO	NDI	O	F	Output	—	—	—		
PJ[13]	PCR[157]]	AF0	SWCLK	SWD	I	M	Input	—	—	—		
PJ[14]	PCR[158]]	AF0	SWIO	SWD	I/O	M	Tristate	—	—	—		

¹ Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIUL module.

PCR.PA = 00→ AF0; PCR.PA = 01 -> AF1; PCR.PA = 10 -> AF2; PCR.PA = 11-> AF3. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".

² Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.

³ The RESET configuration applies during and after reset.

⁴ 100LQFP refers to CCFC2017BC90L3; 144LQFP refers to CCFC2017BC90L5; 176LQFP refers to CCFC2017BC90L7.

⁵ All WKPU pins also support external interrupt capability. See the WKPU chapter for further details.

⁶ NMI has higher priority than alternate function. When NMI is selected, the PCR.AF field is ignored.

⁷ "Not applicable" because these functions are available only while the device is booting. Refer to the BAM information for details.

⁸ Value of PCR.IBE bit must be 0

⁹ This wakeup input cannot be used to exit STANDBY mode.

¹⁰ Out of reset all the functional pins except PC[0:1] and PH[9:10] are available to the user as GPIO.

PC[0:1] are available as JTAG pins (TDI and TDO respectively). PH[9:10] are available as JTAG pins (TCK and TMS respectively). It is up to the user to configure these pins as GPIO when needed.

¹¹ PC[1] is a fast/medium pad but is in medium configuration by default. This pad is in Alternate Function 2 mode after reset which has TDO functionality. The reset value of PCR.OBE is '1', but this setting has no impact as long as this pad stays in AF2 mode. After configuring this pad as GPIO (PCR.PA = 0), output buffer is enabled as reset value of PCR.OBE = 1.

¹² Not available in 100 LQFP package

3.8 Nexus 2+ pins

Table 6. Nexus 2+ pin descriptions

Port pin	Function	I/O direction	Pad type	Function after reset	Pin number		
					100 LQFP	144 LQFP	
MCKO	Message clock out	O	F	—	—	—	
MDO0	Message data out 0	O	M	—	—	—	
MDO1	Message data out 1	O	M	—	—	—	
MDO2	Message data out 2	O	M	—	—	—	
MDO3	Message data out 3	O	M	—	—	—	
$\overline{\text{EVTI}}$	Event in	I	M	Pull-up	—	—	
$\overline{\text{EVTO}}$	Event out	O	M	—	—	—	
$\overline{\text{MSEO}}$	Message start/end out	O	M	—	—	—	

4 Electrical characteristics

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

4.1 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in [Table 7](#) are used and the parameters are tagged accordingly in the tables where appropriate.

Table 7. Parameter classifications

Classification tag	Tag description
--------------------	-----------------

Electrical characteristics

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4.2 NVUSRO register

Bit values in the Non-Volatile User Options (NVUSRO) Register control portions of the device configuration, namely electrical parameters such as high voltage supply and oscillator margin, as well as digital functionality (watchdog enable/disable after reset).

For a detailed description of the NVUSRO register, please refer to the device reference manual.

4.2.1 NVUSRO[**PAD3V5V**] field description

The DC electrical characteristics are dependent on the PAD3V5V bit value. [Table 8](#) shows how NVUSRO[**PAD3V5V**] controls the device configuration.

Table 8. PAD3V5V field description¹

Value ²	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

¹ See the device reference manual for more information on the NVUSRO register.

² Default manufacturing value is ‘1’. Value can be programmed by customer in Shadow Flash.

4.2.2 NVUSRO[**WATCHDOG_EN**] field description

The watchdog enable/disable configuration after reset is dependent on the WATCHDOG_EN bit value. [Table 10](#) shows how NVUSRO[**WATCHDOG_EN**] controls the device configuration.

Table 10. WATCHDOG_EN field description

Value ¹	Description
0	Disable after reset
1	Enable after reset

¹ Default manufacturing value is ‘1’. Value can be programmed by customer in Shadow Flash.

4.3 Absolute maximum ratings

Table 11. Absolute maximum ratings

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	-0.3	6.0	V
V_{SS_LV}	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	$V_{SS} - 0.1$	$V_{SS} + 0.1$	V
V_{DD_BV}	SR	Voltage on VDD_BV (regulator supply) pin with respect to ground (V_{SS})	—	-0.3	6.0	V
			Relative to V_{DD}	-0.3	$V_{DD} + 0.3$	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pins with respect to ground (V_{SS})	—	$V_{SS} - 0.1$	$V_{SS} + 0.1$	V
V_{DD_ADC}	SR	Voltage on VDD_HV_ADC0, VDD_HV_ADC1 (ADC reference) pins with respect to ground (V_{SS})	—	-0.3	6.0	V
			Relative to V_{DD}	$V_{DD} - 0.3$	$V_{DD} + 0.3$	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	-0.3	6.0	V
			Relative to V_{DD}	—	$V_{DD} + 0.3$	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	-10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	-50	50	
I_{AVGSEG}	SR	Sum of all the static I/O current within a supply segment	$V_{DD} = 5.0\text{ V} \pm 10\%$, $PAD3V5V = 0$	—	70	mA
			$V_{DD} = 3.3\text{ V} \pm 10\%$, $PAD3V5V = 1$	—	64	
$T_{STORAGE}$	SR	Storage temperature	—	-55	150	°C

NOTE

Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

4.4 Recommended operating conditions

Table 12. Recommended operating conditions (3.3 V)

Symbol	Parameter	Conditions	Value		Unit	
			Min	Max		
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}^1	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	3.0	3.6	V
$V_{SS_LV}^2$	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	$V_{SS} - 0.1$	$V_{SS} + 0.1$	V
$V_{DD_BV}^3$	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	3.0	3.6	V
			Relative to V	$V_{DD} - 0.1$	$V_{DD} + 0.1$	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS})	—	$V_{SS} - 0.1$	$V_{SS} + 0.1$	V
$V_{DD_ADC}^4$	SR	Voltage on VDD_HV_ADC0, VDD_HV_ADC1 (ADC reference) with respect to ground (V_{SS})	—	3.0^5	3.6	V
			Relative to V_{DD}	$V_{DD} - 0.1$	$V_{DD} + 0.1$	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	$V_{SS} - 0.1$	—	V
			Relative to V_{DD}	—	$V_{DD} + 0.1$	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	-5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	-50	50	
TV_{DD}	SR	V_{DD} slope to ensure correct power up ⁶	—	3.0^7	0.25 V/ μ s	V/s
T_A	SR	Ambient temperature under bias	$f_{CPU} \leq 300\text{MHz}^8$	-40	125	°C
T_J	SR	Junction temperature under bias	—	-40	150	

¹ 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.

² 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.

³ 470 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics). Supply ramp slope on V_{DD_BV} should always be faster or equal to slope of V_{DD_HV} . Otherwise, device may enter regulator bypass mode if slope on V_{DD_BV} is slower.

⁴ 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.

⁵ Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed. When voltage drops below V_{LVDHVL} , device is reset.

⁶ Guaranteed by device validation

⁷ Minimum value of TV_{DD} must be guaranteed until V_{DD} reaches 2.6 V (maximum value of V_{PORH})

⁸ When the FMPLL uses the frequency modulation with a modulation depth of 4% from the center spread frequency, the maximum value of f_{CPU} is 300MHz.

Table 13. Recommended operating conditions (5.0 V)

Symbol	Parameter	Conditions	Value		Unit	
			Min	Max		
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}^1	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	4.5	5.5	V
		Voltage drop ²		3.0	5.5	
$V_{SS_LV}^3$	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	$V_{SS} - 0.1$	$V_{SS} + 0.1$	V
$V_{DD_BV}^4$	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	4.5	5.5	V
		Voltage drop ²		3.0	5.5	
		Relative to V_{DD}		3.0	$V_{DD} + 0.1$	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS})	—	$V_{SS} - 0.1$	$V_{SS} + 0.1$	V
$V_{DD_ADC}^5$	SR	Voltage on VDD_HV_ADC0, VDD_HV_ADC1 (ADC reference) with respect to ground (V_{SS})	—	4.5	5.5	V
		Voltage drop ²		3.0	5.5	
		Relative to V_{DD}		$V_{DD} - 0.1$	$V_{DD} + 0.1$	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	$V_{SS} - 0.1$	—	V
		Relative to V		—	$V_{DD} + 0.1$	
I_{INPAD}	SR	Injected input current on any pin during overload condition	—	-5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	-50	50	
TV_{DD}	SR	V_{DD} slope to ensure correct power up ⁶	—	3.0^7	$0.25 \text{ V}/\mu\text{s}$	V/s
T_A M-Grade Part	SR	Ambient temperature under bias	$f_{CPU} \leq 300\text{MHz}^8$	-40	125	°C
T_J M-Grade Part	SR	Junction temperature under bias	—	-40	150	

¹ 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.

² Full device operation is guaranteed by design when the voltage drops below 4.5 V down to 3.0 V. However, certain analog electrical characteristics will not be guaranteed to stay within the stated limits.

³ 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.

⁴ 470 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics). While the supply voltage ramps up, the slope on V_{DD_BV} should be less than $0.9V_{DD_HV}$ in order to ensure the device does not enter regulator bypass mode.

⁵ 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.

⁶ Guaranteed by device validation

⁷ Minimum value of TV_{DD} must be guaranteed until V_{DD} reaches 2.6 V (maximum value of V_{PORH})

⁸ When the FMPLL uses the frequency modulation with a modulation depth of 4% from the center spread frequency, the maximum value of f_{CPU} is 300MHz.

NOTE

RAM data retention is guaranteed with V_{DD_LV} not below 1.08 V.

4.5 Thermal characteristics

4.5.1 External ballast resistor recommendations

External ballast resistor on V_{DD_BV} pin helps in reducing the overall power dissipation inside the device. This resistor is required only when maximum power consumption exceeds the limit imposed by package thermal characteristics.

As stated in [Table 14](#) LQFP thermal characteristics, considering a thermal resistance of 144 LQFP as 48.3 °C/W, at ambient temperature $T_A = 125$ °C, the junction temperature T_j will cross 150 °C if the total power dissipation is greater than $(150 - 125)/48.3 = 517$ mW. Therefore, the total device current I_{DDMAX} at 125 °C/5.5 V must not exceed 94.1 mA (i.e., PD/VDD). Assuming an average $I_{DD}(V_{DD_HV})$ of 15–20 mA consumption typically during device RUN mode, the LV domain consumption $I_{DD}(V_{DD_BV})$ is thus limited to $I_{DDMAX} - I_{DD}(V_{DD_HV})$, i.e., 80 mA.

Therefore, respecting the maximum power allowed as explained in [4.5.2, Package thermal characteristics](#), it is recommended to use this resistor only in the 125 °C/5.5 V operating corner as per the following guidelines:

- If $I_{DD}(V_{DD_BV}) < 80$ mA, then no resistor is required.
- If $80 \text{ mA} < I_{DD}(V_{DD_BV}) < 90$ mA, then 4 Ω resistor can be used.
- If $I_{DD}(V_{DD_BV}) > 90$ mA, then 8 Ω resistor can be used.

Using resistance in the range of 4–8 Ω, the gain will be around 10–20% of total consumption on V_{DD_BV} . For example, if 8 Ω resistor is used, then power consumption when $I_{DD}(V_{DD_BV})$ is 110 mA is equivalent to power consumption when $I_{DD}(V_{DD_BV})$ is 90 mA (approximately) when resistor not used.

In order to ensure correct power up, the minimum V_{DD_BV} to be guaranteed is 30 mV. If the supply ramp is slower than this value, then LVDHV3B monitoring ballast supply V_{DD_BV} pin gets triggered leading to device reset. Until the supply reaches certain threshold, this low voltage detector (LVD) generates destructive reset event in the system. This threshold depends on the maximum $I_{DD}(V_{DD_BV})$ possible across the external resistor.

4.5.2 Package thermal characteristics

Table 14. LQFP thermal characteristics¹

Symbol	C	Parameter	Conditions ²	Pin count	Value			Unit
					Min	Typ	Max	
R _{θJA}	CC	D Thermal resistance, junction-to-ambient natural convection ³	Single-layer board — 1s	100	—	—	64	°C/W
				144	—	—	64	
				176	—	—	64	
			Four-layer board — 2s2p	100	—	—	49.7	
				144	—	—	48.3	
				176	—	—	47.3	

Table 14. LQFP thermal characteristics¹ (continued)

Symbol	C	Parameter	Conditions ²	Pin count	Value			Unit
					Min	Typ	Max	
R _{θJB}	CC	Thermal resistance, junction-to-board ⁴	Single-layer board — 1s	100	—	—	36	°C/W
				144	—	—	38	
				176	—	—	38	
			Four-layer board — 2s2p	100	—	—	33.6	
				144	—	—	33.4	
				176	—	—	33.4	
R _{θJC}	CC	Thermal resistance, junction-to-case ⁵	Single-layer board — 1s	100	—	—	23	°C/W
				144	—	—	23	
				176	—	—	23	
			Four-layer board — 2s2p	100	—	—	19.8	
				144	—	—	19.2	
				176	—	—	18.8	

¹ Thermal characteristics are targets based on simulation.

² V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C.

³ Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package. When Greek letters are not available, the symbols are typed as R_{thJA} and R_{thJMA}.

⁴ Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. When Greek letters are not available, the symbols are typed as R_{thJB}.

⁵ Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer. When Greek letters are not available, the symbols are typed as R_{thJC}.

4.5.3 Power considerations

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using [Equation 1](#):

$$T_J = T_A + (P_D \times R_{\theta JA}) \quad \text{Eqn. 1}$$

Where:

T_A is the ambient temperature in °C.

R_{θJA} is the package junction-to-ambient thermal resistance, in °C/W.

P_D is the sum of P_{INT} and P_{I/O} (P_D = P_{INT} + P_{I/O}).

P_{INT} is the product of I_{DD} and V_{DD}, expressed in watts. This is the chip internal power.

P_{I/O} represents the power dissipation on input and output pins; user determined.

Most of the time for the applications, P_{I/O} < P_{INT} and may be neglected. On the other hand, P_{I/O} may be significant, if the device is configured to continuously drive external modules and/or memories.

Electrical characteristics

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273 \text{ }^\circ\text{C}) \quad \text{Eqn. 2}$$

Therefore, solving equations 1 and 2:

$$K = P_D \times (T_A + 273 \text{ }^\circ\text{C}) + R_{\theta JA} \times P_D^2 \quad \text{Eqn. 3}$$

Where:

K is a constant for the particular part, which may be determined from [Equation 3](#) by measuring P_D (at equilibrium) for a known T_A . Using this value of K , the values of P_D and T_J may be obtained by solving equations 1 and 2 iteratively for any value of T_A .

4.6 I/O pad electrical characteristics

4.6.1 I/O pad types

The device provides four main I/O pad types depending on the associated alternate functions:

- Slow pads—are the most common pads, providing a good compromise between transition time and low electromagnetic emission.
- Medium pads—provide transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
- Fast pads—provide maximum speed. These are used for improved Nexus debugging capability.
- Input only pads—are associated with ADC channels and 32 kHz low power external crystal oscillator providing low input leakage.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance.

4.6.2 I/O input DC characteristics

[Table 15](#) provides input DC electrical characteristics as described in [Figure 6](#).

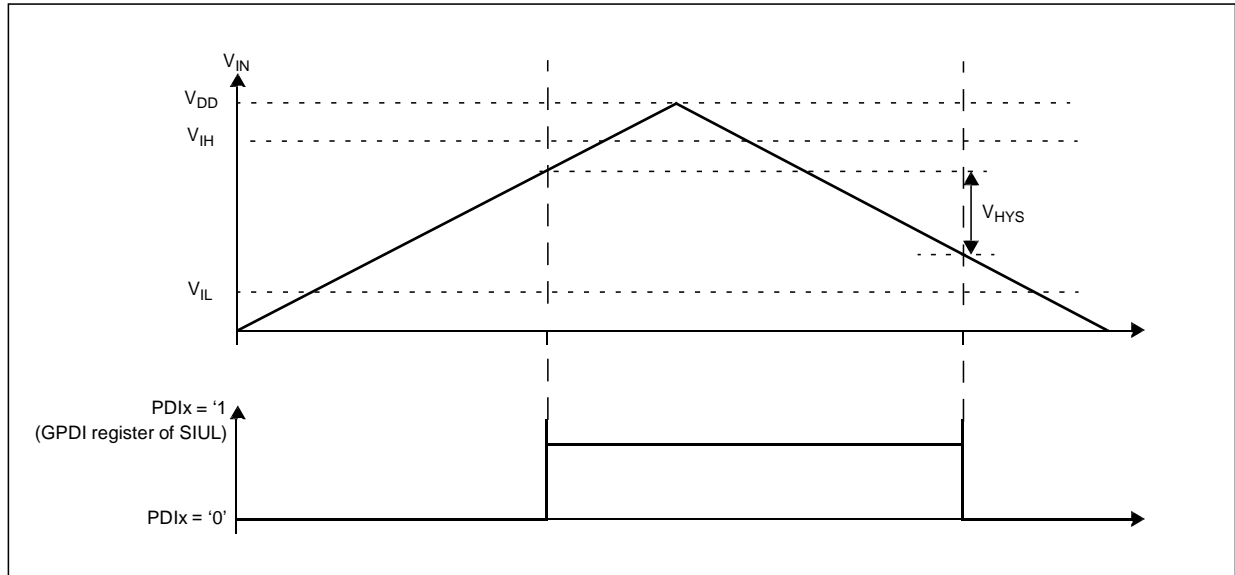


Figure 6. I/O input DC electrical characteristics definition

Table 15. I/O input DC electrical characteristics

Symbol	C	Parameter	Conditions ¹	Value			Unit		
				Min	Typ	Max			
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	—	0.65 V_{DD}	—	$V_{DD} + 0.4$	V	
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	—	-0.4	—	0.35 V_{DD}	V	
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—	0.1 V_{DD}	—	—	V	
I_{LKG}	CC	D	Digital input leakage	No injection on adjacent pin	$T_A = -40\text{ }^\circ\text{C}$	—	2	200	nA
					$T_A = 25\text{ }^\circ\text{C}$	—	2	200	
					$T_A = 85\text{ }^\circ\text{C}$	—	5	300	
					$T_A = 105\text{ }^\circ\text{C}$	—	12	500	
					$T_A = 125\text{ }^\circ\text{C}$	—	70	1000	
W_{FI}^2	SR	P	Wakeup input filtered pulse	—	—	—	40	ns	
W_{NFI}^2	SR	P	Wakeup input not filtered pulse	—	1000	—	—	ns	

¹ $V_{DD} = 3.3\text{ V} \pm 10\% / 5.0\text{ V} \pm 10\%$, $T_A = -40$ to $125\text{ }^\circ\text{C}$, unless otherwise specified

² In the range from 40 to 1000 ns, pulses can be filtered or not filtered, according to operating temperature and voltage.

4.6.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- [Table 16](#) provides weak pull figures. Both pull-up and pull-down resistances are supported.

Electrical characteristics

- [Table 17](#) provides output driver characteristics for I/O pads when in SLOW configuration.
- [Table 18](#) provides output driver characteristics for I/O pads when in MEDIUM configuration.
- [Table 19](#) provides output driver characteristics for I/O pads when in FAST configuration.

Table 16. I/O pull-up/pull-down DC electrical characteristics

Symbol	C	Parameter	Conditions ¹	Value			Unit		
				Min	Typ	Max			
I _{WPU}	CC	P	Weak pull-up current absolute value	V _{IN} = V _{IL} , V _{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	μA
					PAD3V5V = 1 ²	10	—	250	
				V _{IN} = V _{IL} , V _{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	
I _{WPD}	CC	P	Weak pull-down current absolute value	V _{IN} = V _{IH} , V _{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	μA
					PAD3V5V = 1	10	—	250	
				V _{IN} = V _{IH} , V _{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

² The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 17. SLOW configuration output buffer electrical characteristics

Symbol	C	Parameter	Conditions ¹	Value			Unit			
				Min	Typ	Max				
V _{OH}	CC	P	Output high level SLOW configuration	Push Pull	I _{OH} = -2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	0.8V _{DD}	—	—	V	
						I _{OH} = -2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ²	0.8V _{DD}	—		—
						I _{OH} = -1 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V _{DD} - 0.8	—		—
V _{OL}	CC	P	Output low level SLOW configuration	Push Pull	I _{OL} = 2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	0.1V _{DD}	V	
						I _{OL} = 2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ²	—	—		0.1V _{DD}
						I _{OL} = 1 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—		0.5

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² The configuration PAD3V5 = 1 when $V_{DD} = 5\text{ V}$ is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 18. MEDIUM configuration output buffer electrical characteristics

Symbol	C	Parameter	Conditions ¹	Value			Unit	
				Min	Typ	Max		
V _{OH}	CC	Output high level MEDIUM configuration	Push Pull	I _{OH} = -3.8 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	0.8V _{DD}	—	—	V
				I _{OH} = -2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	0.8V _{DD}	—	—	
				I _{OH} = -1 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ²	0.8V _{DD}	—	—	
				I _{OH} = -1 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V _{DD} - 0.8	—	—	
				I _{OH} = -100 µA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	0.8V _{DD}	—	—	
V _{OL}	CC	Output low level MEDIUM configuration	Push Pull	I _{OL} = 3.8 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	0.2V _{DD}	V
				I _{OL} = 2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	0.1V _{DD}	
				I _{OL} = 1 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ²	—	—	0.1V _{DD}	
				I _{OL} = 1 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
				I _{OL} = 100 µA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	0.1V _{DD}	

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² The configuration PAD3V5 = 1 when $V_{DD} = 5\text{ V}$ is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 19. FAST configuration output buffer electrical characteristics

Symbol	C	Parameter	Conditions ¹	Value			Unit				
				Min	Typ	Max					
V _{OH}	CC	P	Output high level FAST configuration	Push Pull	I _{OH} = -14 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	0.8V _{DD}	—	—	V		
						C	I _{OH} = -7 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ²	0.8V _{DD}		—	—
							C	I _{OH} = -11 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)		V _{DD} - 0.8	—
V _{OL}	CC	P	Output low level FAST configuration	Push Pull	I _{OL} = 14 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	0.1V _{DD}	V		
						C	I _{OL} = 7 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ²	—		—	0.1V _{DD}
							C	I _{OL} = 11 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)		—	—

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

4.6.4 Output pin transition times

Table 20. Output pin transition times

Symbol	C	Parameter	Conditions ¹	Value			Unit				
				Min	Typ	Max					
t _{tr}	CC	D	Output transition time output pin ² SLOW configuration	C _L = 25 pF	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns		
						T	C _L = 50 pF	—		—	100
							D	C _L = 100 pF		—	—
	D	T	D	C _L = 25 pF	V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50			
						T	C _L = 50 pF	—		—	100
						D	C _L = 100 pF	—		—	125

Table 20. Output pin transition times (continued)

Symbol	C	Parameter	Conditions ¹		Value			Unit	
					Min	Typ	Max		
t_{tr}	CC	Output transition time output pin ² MEDIUM configuration	$C_L = 25$ pF	$V_{DD} = 5.0$ V \pm 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns	
			$C_L = 50$ pF		—	—	20		
			$C_L = 100$ pF		—	—	40		
	D		$C_L = 25$ pF	$V_{DD} = 3.3$ V \pm 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12		
			$C_L = 50$ pF		—	—	25		
			$C_L = 100$ pF		—	—	40		
t_{tr}	CC	Output transition time output pin ² FAST configuration	$C_L = 25$ pF	$V_{DD} = 5.0$ V \pm 10%, PAD3V5V = 0	—	—	4	ns	
			$C_L = 50$ pF		—	—	6		
			$C_L = 100$ pF		—	—	12		
			D	$C_L = 25$ pF	$V_{DD} = 3.3$ V \pm 10%, PAD3V5V = 1	—	—		4
				$C_L = 50$ pF		—	—		7
				$C_L = 100$ pF		—	—		12

¹ $V_{DD} = 3.3$ V \pm 10% / 5.0 V \pm 10%, $T_A = -40$ to 125 °C, unless otherwise specified

² C_L includes device and package capacitances ($C_{PKG} < 5$ pF).

4.6.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in Table 21.

Table 22 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

Table 21. I/O supply segments

Package	Supply segment							
	1	2	3	4	5	6	7	8
176 LQFP	pin7 – pin27	pin28 – pin57	pin59 – pin85	pin86 – pin123	pin124 – pin150	pin151 – pin6	—	—
144 LQFP	pin20 – pin49	pin51 – pin99	pin100 – pin122	pin 123 – pin19	—	—	—	—
100 LQFP	pin16 – pin35	pin37 – pin69	pin70 – pin83	pin84 – pin15	—	—	—	—

Table 22. I/O consumption

Symbol	C	Parameter	Conditions ¹		Value			Unit	
					Min	Typ	Max		
I _{SWTSLW} ²	CC	D	Dynamic I/O current for SLOW configuration	C _L = 25 pF	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	mA
					V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16	
I _{SWTMED} ²	CC	D	Dynamic I/O current for MEDIUM configuration	C _L = 25 pF	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	29	mA
					V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	17	
I _{SWTFST} ²	CC	D	Dynamic I/O current for FAST configuration	C _L = 25 pF	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	110	mA
					V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
I _{RMSLW}	CC	D	Root mean square I/O current for SLOW configuration	C _L = 25 pF, 2 MHz	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.3	mA
				C _L = 25 pF, 4 MHz		—	—	3.2	
				C _L = 100 pF, 2 MHz		—	—	6.6	
				C _L = 25 pF, 2 MHz	V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.6	
				C _L = 25 pF, 4 MHz		—	—	2.3	
				C _L = 100 pF, 2 MHz		—	—	4.7	
I _{RMSMED}	CC	D	Root mean square I/O current for MEDIUM configuration	C _L = 25 pF, 13 MHz	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.6	mA
				C _L = 25 pF, 40 MHz		—	—	13.4	
				C _L = 100 pF, 13 MHz		—	—	18.3	
				C _L = 25 pF, 13 MHz	V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	5	
				C _L = 25 pF, 40 MHz		—	—	8.5	
				C _L = 100 pF, 13 MHz		—	—	11	
I _{RMSFST}	CC	D	Root mean square I/O current for FAST configuration	C _L = 25 pF, 40 MHz	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	22	mA
				C _L = 25 pF, 64 MHz		—	—	33	
				C _L = 100 pF, 40 MHz		—	—	56	
				C _L = 25 pF, 40 MHz	V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14	
				C _L = 25 pF, 64 MHz		—	—	20	
				C _L = 100 pF, 40 MHz		—	—	35	
I _{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V _{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

Table 23 provides the weight of concurrent switching I/Os.

Due to the dynamic current limitations, the sum of the weight of concurrent switching I/Os on a single segment must not exceed 100% to ensure device functionality.

Table 23. I/O weight¹

Supply segment			Pad	176 LQFP				144/100 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
176 LQFP	144 LQFP	100 LQFP		SRC ² = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
6	4	4	PB[3]	5%	—	6%	—	13%	—	15%	—
			PC[9]	4%	—	5%	—	13%	—	15%	—
			PC[14]	4%	—	4%	—	13%	—	15%	—
			PC[15]	3%	4%	4%	4%	12%	18%	15%	16%
			PJ[4]	3%	4%	3%	3%	—	—	—	—
1	—	—	PH[15]	2%	3%	3%	3%	—	—	—	—
	—	—	PH[13]	3%	4%	3%	4%	—	—	—	—
	—	—	PH[14]	3%	4%	4%	4%	—	—	—	—
	—	—	PI[6]	4%	—	4%	—	—	—	—	—
	—	—	PI[7]	4%	—	4%	—	—	—	—	—
	4	—	PG[5]	4%	—	5%	—	10%	—	12%	—
		—	PG[4]	4%	6%	5%	5%	9%	13%	11%	12%
		—	PG[3]	4%	—	5%	—	9%	—	11%	—
		—	PG[2]	4%	6%	5%	5%	9%	12%	10%	11%
	4	4	PA[2]	4%	—	5%	—	8%	—	10%	—
			PE[0]	4%	—	5%	—	8%	—	9%	—
			PA[1]	4%	—	5%	—	8%	—	9%	—
			PE[1]	4%	6%	5%	6%	7%	10%	9%	9%
			PE[8]	4%	6%	5%	6%	7%	10%	8%	9%
			PE[9]	4%	—	5%	—	6%	—	8%	—
PE[10]			4%	—	5%	—	6%	—	7%	—	
PA[0]			4%	6%	5%	5%	6%	8%	7%	7%	
PE[11]	4%	—	5%	—	5%	—	6%	—			

Table 23. I/O weight¹ (continued)

Supply segment			Pad	176 LQFP				144/100 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
176 LQFP	144 LQFP	100 LQFP		SRC ² = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
2	1	—	PG[9]	9%	—	10%	—	9%	—	10%	—
		—	PG[8]	9%	—	11%	—	9%	—	11%	—
		1	PC[11]	9%	—	11%	—	9%	—	11%	—
			PC[10]	9%	13%	11%	12%	9%	13%	11%	12%
		—	PG[7]	9%	—	11%	—	9%	—	11%	—
		—	PG[6]	10%	14%	11%	12%	10%	14%	11%	12%
		1	PB[0]	10%	14%	12%	12%	10%	14%	12%	12%
			PB[1]	10%	—	12%	—	10%	—	12%	—
		—	PF[9]	10%	—	12%	—	10%	—	12%	—
		—	PF[8]	10%	14%	12%	13%	10%	14%	12%	13%
		—	PF[12]	10%	15%	12%	13%	10%	15%	12%	13%
		1	PC[6]	10%	—	12%	—	10%	—	12%	—
			PC[7]	10%	—	12%	—	10%	—	12%	—
		—	PF[10]	10%	14%	11%	12%	10%	14%	11%	12%
		—	PF[11]	9%	—	11%	—	9%	—	11%	—
		1	PA[15]	8%	12%	10%	10%	8%	12%	10%	10%
		—	PF[13]	8%	—	10%	—	8%	—	10%	—
		1	PA[14]	8%	11%	9%	10%	8%	11%	9%	10%
			PA[4]	7%	—	9%	—	7%	—	9%	—
			PA[13]	7%	10%	8%	9%	7%	10%	8%	9%
PA[12]	7%		—	8%	—	7%	—	8%	—		

Table 23. I/O weight¹ (continued)

Supply segment			Pad	176 LQFP				144/100 LQFP				
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V		
176 LQFP	144 LQFP	100 LQFP		SRC ² = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	
3	2	2	PB[9]	1%	—	1%	—	1%	—	1%	—	
			PB[8]	1%	—	1%	—	1%	—	1%	—	
			PB[10]	5%	—	6%	—	6%	—	7%	—	
		—	PF[0]	5%	—	6%	—	6%	—	8%	—	
		—	PF[1]	5%	—	6%	—	7%	—	8%	—	
		—	PF[2]	6%	—	7%	—	7%	—	9%	—	
		—	PF[3]	6%	—	7%	—	8%	—	9%	—	
		—	PF[4]	6%	—	7%	—	8%	—	10%	—	
		—	PF[5]	6%	—	7%	—	9%	—	10%	—	
		—	PF[6]	6%	—	7%	—	9%	—	11%	—	
	—	PF[7]	6%	—	7%	—	9%	—	11%	—		
	—	—	PJ[3]	6%	—	7%	—	—	—	—	—	
	—	—	PJ[2]	6%	—	7%	—	—	—	—	—	
	—	—	PJ[1]	6%	—	7%	—	—	—	—	—	
	—	—	PJ[0]	6%	—	7%	—	—	—	—	—	
	—	—	PI[15]	6%	—	7%	—	—	—	—	—	
	—	—	PI[14]	6%	—	7%	—	—	—	—	—	
	—	2	2	PD[0]	1%	—	1%	—	1%	—	1%	—
	—			PD[1]	1%	—	1%	—	1%	—	1%	—
—	PD[2]			1%	—	1%	—	1%	—	1%	—	
—	PD[3]			1%	—	1%	—	1%	—	1%	—	
—	PD[4]			1%	—	1%	—	1%	—	1%	—	
—	PD[5]			1%	—	1%	—	1%	—	1%	—	
—	PD[6]			1%	—	1%	—	1%	—	2%	—	
—	PD[7]			1%	—	1%	—	1%	—	2%	—	

Table 23. I/O weight¹ (continued)

Supply segment			Pad	176 LQFP				144/100 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
176 LQFP	144 LQFP	100 LQFP		SRC ² = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
4	2	2	PD[8]	1%	—	1%	—	1%	—	2%	—
			PB[4]	1%	—	1%	—	1%	—	2%	—
			PB[5]	1%	—	1%	—	1%	—	2%	—
			PB[6]	1%	—	1%	—	1%	—	2%	—
			PB[7]	1%	—	1%	—	1%	—	2%	—
			PD[9]	1%	—	1%	—	1%	—	2%	—
			PD[10]	1%	—	1%	—	1%	—	2%	—
			PD[11]	1%	—	1%	—	1%	—	2%	—
4	—	—	PB[11]	1%	—	1%	—	—	—	—	—
	—	—	PD[12]	11%	—	13%	—	—	—	—	—
	2	2	PB[12]	11%	—	13%	—	15%	—	17%	—
			PD[13]	11%	—	13%	—	14%	—	17%	—
			PB[13]	11%	—	13%	—	14%	—	17%	—
			PD[14]	11%	—	13%	—	14%	—	17%	—
			PB[14]	11%	—	13%	—	14%	—	16%	—
			PD[15]	11%	—	13%	—	13%	—	16%	—
			PB[15]	11%	—	13%	—	13%	—	15%	—
	—	—	PI[8]	10%	—	12%	—	—	—	—	—
	—	—	PI[9]	10%	—	12%	—	—	—	—	—
	—	—	PI[10]	10%	—	12%	—	—	—	—	—
	—	—	PI[11]	10%	—	12%	—	—	—	—	—
	—	—	PI[12]	10%	—	12%	—	—	—	—	—
	—	—	PI[13]	10%	—	11%	—	—	—	—	—
	2	2	PA[3]	9%	—	11%	—	11%	—	13%	—
			PG[13]	9%	13%	11%	11%	10%	14%	12%	13%
			PG[12]	9%	13%	10%	11%	10%	14%	12%	12%
			PH[0]	6%	8%	7%	7%	6%	9%	7%	8%
			PH[1]	6%	8%	7%	7%	6%	8%	7%	7%
PH[2]			5%	7%	6%	6%	5%	7%	6%	7%	
PH[3]			5%	7%	5%	6%	5%	7%	6%	6%	
PG[1]			4%	—	5%	—	4%	—	5%	—	
PG[0]			4%	5%	4%	5%	4%	5%	4%	5%	

Table 23. I/O weight¹ (continued)

Supply segment			Pad	176 LQFP				144/100 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
176 LQFP	144 LQFP	100 LQFP		SRC ² = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
5	3	—	PF[15]	4%	—	4%	—	4%	—	4%	—
		—	PF[14]	4%	6%	5%	5%	4%	6%	5%	5%
		—	PE[13]	4%	—	5%	—	4%	—	5%	—
		3	PA[7]	5%	—	6%	—	5%	—	6%	—
			PA[8]	5%	—	6%	—	5%	—	6%	—
			PA[9]	6%	—	7%	—	6%	—	7%	—
			PA[10]	6%	—	8%	—	6%	—	8%	—
			PA[11]	8%	—	9%	—	8%	—	9%	—
			PE[12]	8%	—	9%	—	8%	—	9%	—
		—	PG[14]	8%	—	9%	—	8%	—	9%	—
		—	PG[15]	8%	11%	9%	10%	8%	11%	9%	10%
		—	PE[14]	8%	—	9%	—	8%	—	9%	—
		—	PE[15]	8%	11%	9%	10%	8%	11%	9%	10%
	—	PG[10]	8%	—	9%	—	8%	—	9%	—	
	—	PG[11]	7%	11%	9%	9%	7%	11%	9%	9%	
	—	—	PH[11]	7%	10%	9%	9%	—	—	—	—
	—	—	PH[12]	7%	10%	8%	9%	—	—	—	—
	—	—	PI[5]	7%	—	8%	—	—	—	—	—
	—	—	PI[4]	7%	—	8%	—	—	—	—	—
	3	3	PC[3]	6%	—	8%	—	6%	—	8%	—
PC[2]			6%	8%	7%	7%	6%	8%	7%	7%	
PA[5]			6%	8%	7%	7%	6%	8%	7%	7%	
PA[6]			5%	—	6%	—	5%	—	6%	—	
PH[10]			5%	7%	6%	6%	5%	7%	6%	6%	
PC[1]			5%	19%	5%	13%	5%	19%	5%	13%	

Table 23. I/O weight¹ (continued)

Supply segment			Pad	176 LQFP				144/100 LQFP					
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V			
176 LQFP	144 LQFP	100 LQFP		SRC ² = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1		
6	4	4	PC[0]	6%	9%	7%	8%	7%	10%	8%	8%		
			PH[9]	7%	—	8%	—	7%	—	9%	—		
			PE[2]	7%	10%	8%	9%	8%	11%	9%	10%		
			PE[3]	7%	10%	9%	9%	8%	12%	10%	10%		
			PC[5]	7%	11%	9%	9%	8%	12%	10%	11%		
			PC[4]	8%	11%	9%	10%	9%	13%	10%	11%		
			PE[4]	8%	11%	9%	10%	9%	13%	11%	12%		
			PE[5]	8%	11%	10%	10%	9%	14%	11%	12%		
		—	—	—	PH[4]	8%	12%	10%	10%	10%	14%	12%	12%
		—	—	—	PH[5]	8%	—	10%	—	10%	—	12%	—
		—	—	—	PH[6]	8%	12%	10%	11%	10%	15%	12%	13%
		—	—	—	PH[7]	9%	12%	10%	11%	11%	15%	13%	13%
		—	—	—	PH[8]	9%	12%	10%	11%	11%	16%	13%	14%
		—	—	4	PE[6]	9%	12%	10%	11%	11%	16%	13%	14%
		—	—	4	PE[7]	9%	12%	10%	11%	11%	16%	14%	14%
		—	—	—	PI[3]	9%	—	10%	—	—	—	—	—
		—	—	—	PI[2]	9%	—	10%	—	—	—	—	—
		—	—	—	PI[1]	9%	—	10%	—	—	—	—	—
		—	—	—	PI[0]	9%	—	10%	—	—	—	—	—
		—	4	4	PC[12]	8%	12%	10%	11%	12%	18%	15%	16%
—	4	4	PC[13]	8%	—	10%	—	13%	—	15%	—		
—	4	4	PC[8]	8%	—	10%	—	13%	—	15%	—		
—	4	4	PB[2]	8%	11%	9%	10%	13%	18%	15%	16%		

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² SRC: “Slew Rate Control” bit in SIU_PCRx

4.6.6 RESET electrical characteristics

The device implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

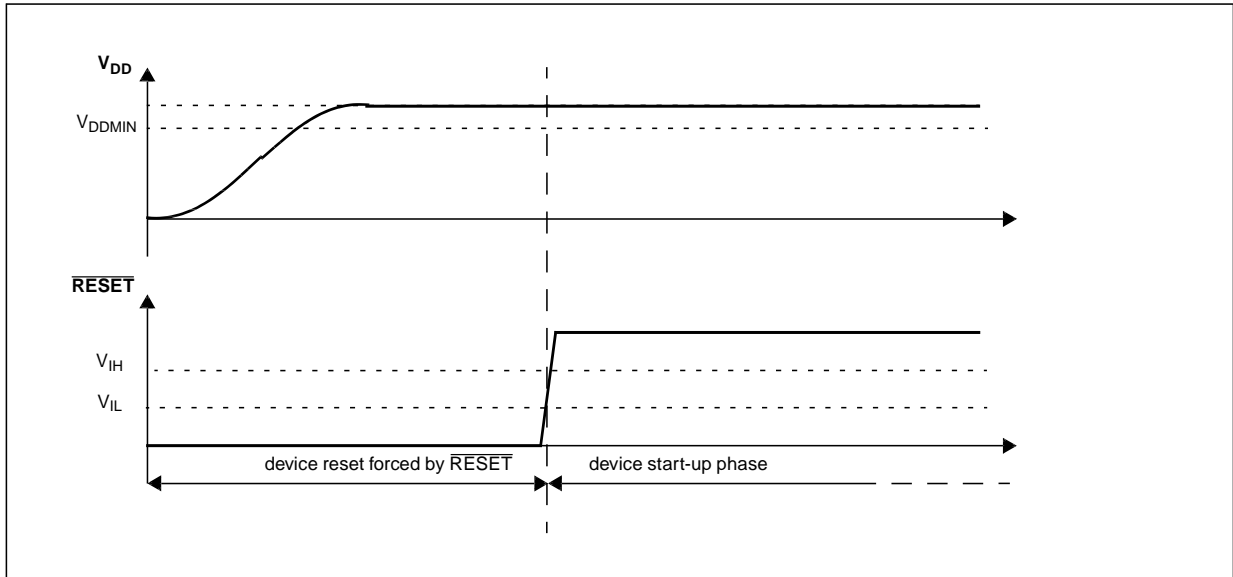


Figure 7. Start-up reset requirements

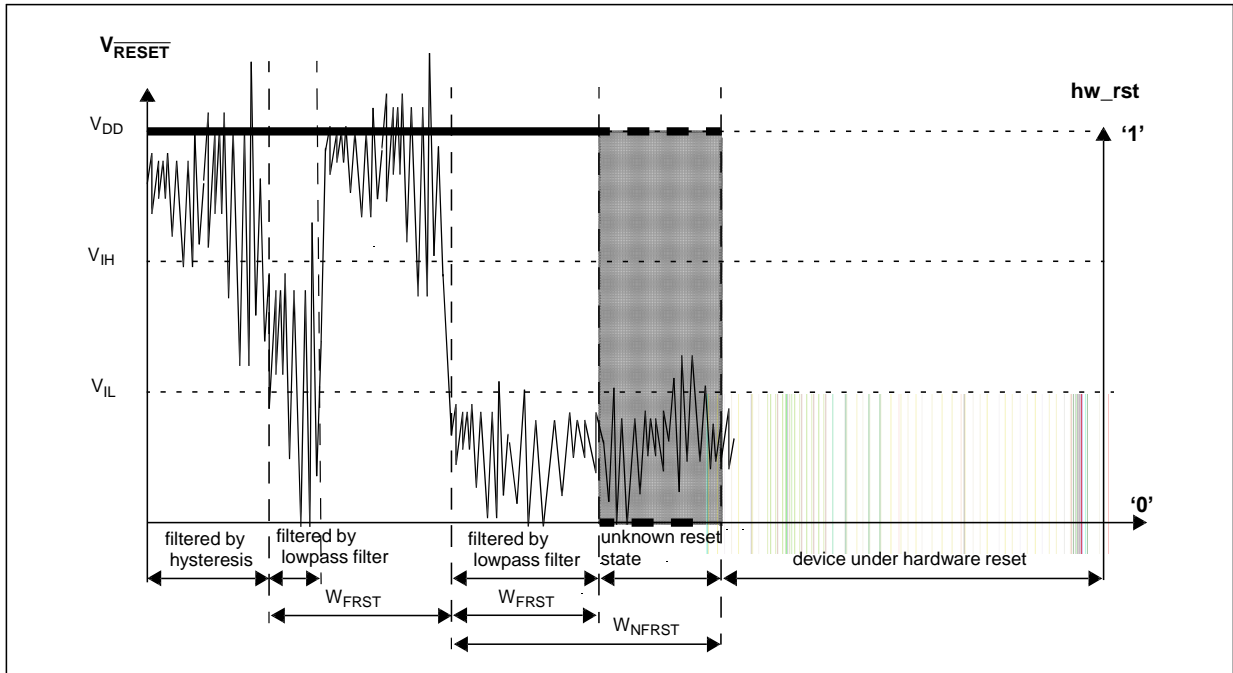


Figure 8. Noise filtering on reset signal

Table 24. Reset electrical characteristics

Symbol	C	Parameter	Conditions ¹	Value			Unit
				Min	Typ	Max	
V _{IH}	SR P	Input High Level CMOS (Schmitt Trigger)	—	0.65V _{DD}	—	V _{DD} + 0.4	V

Electrical characteristics

Table 24. Reset electrical characteristics (continued)

Symbol	C	Parameter	Conditions ¹	Value			Unit	
				Min	Typ	Max		
V _{IL}	SR	P	Input low Level CMOS (Schmitt Trigger)	—	—	0.35V _{DD}	V	
V _{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—	—	0.1V _{DD}	V	
V _{OL}	CC	P	Output low level	Push Pull, I _{OL} = 2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	0.1V _{DD}	V
			Push Pull, I _{OL} = 1 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ²	—	—	0.1V _{DD}		
			Push Pull, I _{OL} = 1 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5		
t _{tr}	CC	D	Output transition time output pin ³ MEDIUM configuration	C _L = 25 pF, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
				C _L = 50 pF, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
				C _L = 100 pF, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
				C _L = 25 pF, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
				C _L = 50 pF, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
				C _L = 100 pF, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
W _{FRST}	SR	P	RESET input filtered pulse	—	—	40	ns	
W _{NFRST}	SR	P	RESET input not filtered pulse	—	1000	—	ns	
I _{WPUL}	CC	P	Weak pull-up current absolute value	V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	10	—	150	μA
		D		V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	10	—	150	
		P		V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ⁴	10	—	250	

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to RGM module section of the device reference manual).

³ C_L includes device and package capacitance (C_{PKG} < 5 pF).

⁴ The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

4.7 Power management electrical characteristics

4.7.1 Voltage regulator electrical characteristics

The device implements an internal voltage regulator to generate the low voltage core supply V_{DD_LV} from the high voltage ballast supply V_{DD_BV} . The regulator itself is supplied by the common I/O supply V_{DD} . The following supplies are involved:

- HV: High voltage external power supply for voltage regulator module. This must be provided externally through V_{DD} power pin.
- BV: High voltage external power supply for internal ballast module. This must be provided externally through V_{DD_BV} power pin. Voltage values should be aligned with V_{DD} .
- LV: Low voltage internal power supply for core, FMPLL and Flash digital logic. This is generated by the internal voltage regulator but provided outside to connect stability capacitor. It is further split into four main domains to ensure noise isolation between critical LV modules within the device:
 - LV_COR: Low voltage supply for the core. It is also used to provide supply for FMPLL through double bonding.
 - LV_CFLA: Low voltage supply for code flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
 - LV_DFLA: Low voltage supply for data flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
 - LV_PLL: Low voltage supply for FMPLL. It is shorted to LV_COR through double bonding.

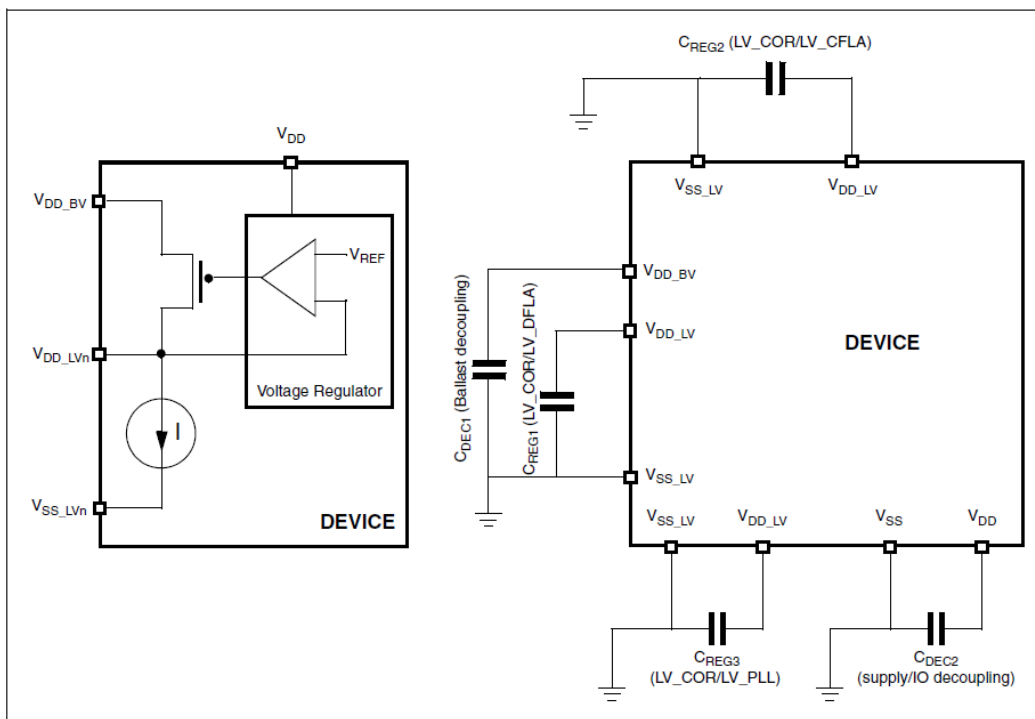


Figure 9. Voltage regulator capacitance connection

The internal voltage regulator requires external capacitance (C_{REGn}) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board

Electrical characteristics
to less than 5 nH.

Each decoupling capacitor must be placed between each of the three V_{DD_LV}/V_{SS_LV} supply pairs to ensure stable voltage (see [4.4, Recommended operating conditions](#)).

Table 25. Voltage regulator electrical characteristics

Symbol	C	Parameter	Conditions ¹	Value			Unit	
				Min	Typ	Max		
C_{REGn}	SR	—	Internal voltage regulator external capacitance	—	200	—	500	nF
R_{REG}	SR	—	Stability capacitor equivalent serial resistance	Range: 10 kHz to 20 MHz	—	—	0.2	Ω
C_{DEC1}	SR	—	Decoupling capacitance ² ballast	V_{DD_BV}/V_{SS_LV} pair: $V_{DD_BV} = 4.5 \text{ V to } 5.5 \text{ V}$	100 ³	470 ⁴	—	nF
				V_{DD_BV}/V_{SS_LV} pair: $V_{DD_BV} = 3 \text{ V to } 3.6 \text{ V}$			400	

Table 25. Voltage regulator electrical characteristics (continued)

Symbol	C	Parameter	Conditions ¹	Value			Unit	
				Min	Typ	Max		
C _{DEC2}	SR	—	Decoupling capacitance regulator supply	V _{DD} /V _{SS} pair	10	100	—	nF
V _{MREG}	CC	T	Main regulator output voltage	Before exiting from reset	—	1.32	—	V
				After trimming	1.08	—	1.25	
I _{MREG}	SR	—	Main regulator current provided to V _{DD_LV} domain	—	—	—	150	mA
I _{MREGINT}	CC	D	Main regulator module current consumption	I _{MREG} = 200 mA	—	—	2	mA
				I _{MREG} = 0 mA	—	—	1	
I _{LPREGINT}	CC	D	Low-power regulator module current consumption	I _{LPREG} = 15 mA; T _A = 55 °C	—	—	600	μA
				I _{LPREG} = 0 mA; T _A = 55 °C	—	5	—	
V _{ULPREG}	CC	P	Ultra low power regulator output voltage	After trimming	1.16	1.28	—	V
I _{ULPREG}	SR	—	Ultra low power regulator current provided to V _{DD_LV} domain	—	—	—	5	mA
I _{ULPREGINT}	CC	D	Ultra low power regulator module current consumption	I _{ULPREG} = 5 mA; T _A = 55 °C	—	—	100	μA
				I _{ULPREG} = 0 mA; T _A = 55 °C	—	2	—	
I _{DD_BV}	CC	D	In-rush average current on V _{DD_BV} during power-up ⁵	—	—	—	300 ⁶	mA

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² This capacitance value is driven by the constraints of the external voltage regulator supplying the V_{DD_BV} voltage. A typical value is in the range of 470 nF.

³ This value is acceptable to guarantee operation from 4.5 V to 5.5 V

⁴ External regulator and capacitance circuitry must be capable of providing I_{DD_BV} while maintaining supply V_{DD_BV} in operating range.

⁵ In-rush average current is seen only for short time during power-up and on standby exit (maximum 20 μs, depending on external capacitances to be loaded).

⁶ The duration of the in-rush current depends on the capacitance placed on LV pins. BV decoupling capacitors must be sized accordingly. Refer to I_{MREG} value for minimum amount of current to be provided in cc.

4.7.2 Low voltage detector electrical characteristics

The device implements a power-on reset (POR) module to ensure correct power-up initialization, as well as five low voltage detectors (LVDs) to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

Electrical characteristics

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state (refer to RGM Destructive Event Status (RGM_DES) Register flag F_POR in device reference manual)
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD27 in device reference manual)
- LVDHV3B monitors V_{DD_BV} to ensure device reset below minimum functional supply (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD27_VREG in device reference manual)
- LVDHV5 monitors V_{DD} when application uses device in the $5.0\text{ V} \pm 10\%$ range (refer to RGM Functional Event Status (RGM_FES) Register flag F_LVD45 in device reference manual)
- LVDLVCOR monitors power domain No. 1 (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD12_PD1 in device reference manual)
- LVDLVBKP monitors power domain No. 0 (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD12_PD0 in device reference manual)

NOTE

When enabled, power domain No. 2 is monitored through LVDLVBKP.

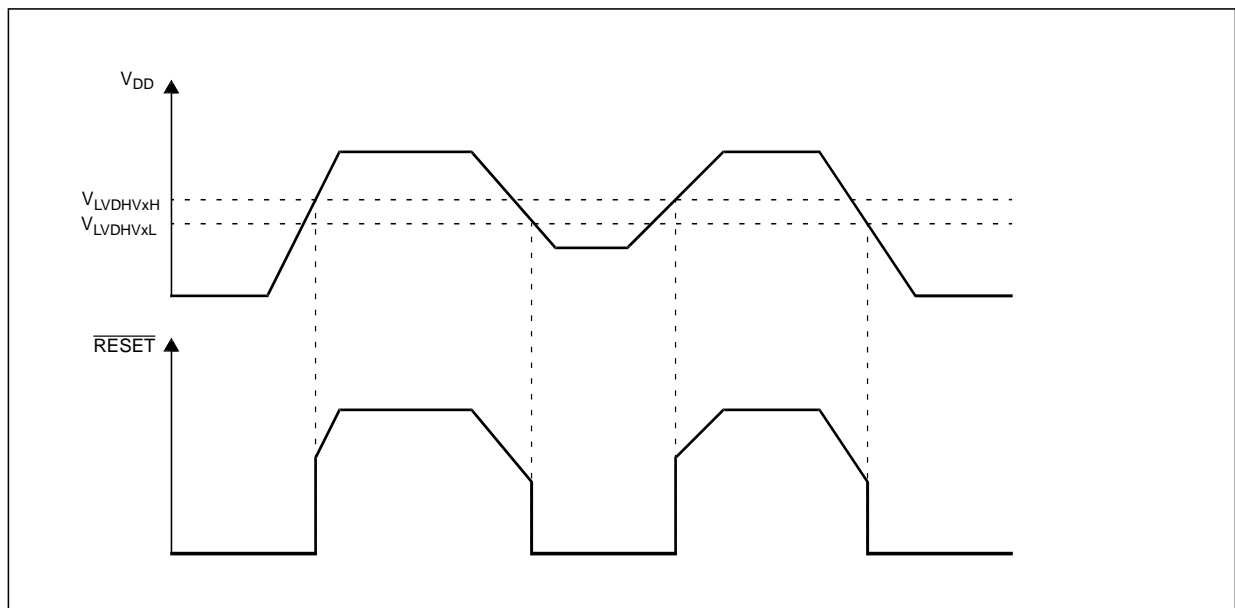


Figure 10. Low voltage detector vs reset

Table 26. Low voltage detector electrical characteristics

Symbol	C	Parameter	Conditions ¹	Value			Unit	
				Min	Typ	Max		
V _{PORUP}	SR	P	T _A = 25 °C, after trimming	1.0	—	5.5	V	
V _{PORH}	CC	P		Power-on reset threshold	1.5	—		2.6
V _{LVDHV3H}	CC	T		LVDHV3 low voltage detector high threshold	—	—		2.95
V _{LVDHV3L}	CC	P		LVDHV3 low voltage detector low threshold	2.6	—		2.9
V _{LVDHV3BH}	CC	P		LVDHV3B low voltage detector high threshold	—	—		2.95
V _{LVDHV3BL}	CC	P		LVDHV3B low voltage detector low threshold	2.6	—		2.9
V _{LVDHV5H}	CC	T		LVDHV5 low voltage detector high threshold	—	—		4.5
V _{LVDHV5L}	CC	P		LVDHV5 low voltage detector low threshold	3.8	—		4.4
V _{LVDLVCORL}	CC	P		LVDLVCOR low voltage detector low threshold	1.08	—		1.16
V _{LVDLVBKPL}	CC	P		LVDLVBKP low voltage detector low threshold	1.08	—		1.16

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

4.8 Power consumption

Table 27 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

Table 27. Power consumption on VDD_BV and VDD_HV

Symbol	C	Parameter	Conditions ¹	Value			Unit		
				Min	Typ	Max			
I _{DDMAX} ²	CC	D	RUN mode maximum average current	—	115	140 ³	mA		
I _{DDRUN} ⁴	CC		RUN mode typical average current ⁵	—	70	125	mA		
I _{DDHALT}	CC	C	HALT mode current ⁶	Slow internal RC oscillator (128 kHz) running	T _A = 25 °C	—	10	18	mA
					T _J = 125 °C	—	17	28	
I _{DDSTOP}	CC	P	STOP mode current ⁷	Slow internal RC oscillator (128 kHz) running	T _A = 25 °C	—	3.5	5	mA
					T _J = 125 °C	—	35	50	
I _{DDSTDBY}	CC	P	STANDBY mode current	Slow internal RC oscillator (128 kHz) running	T _A = 25 °C	—	0.43	0.77	mA
					T _J = 125 °C	—	4.3	7.7	

Electrical characteristics

- ¹ $V_{DD} = 3.3\text{ V} \pm 10\% / 5.0\text{ V} \pm 10\%$, $T_A = -40$ to $125\text{ }^\circ\text{C}$, unless otherwise specified
- ² Running consumption does not include I/Os toggling which is highly dependent on the application. The given value is thought to be a worst case value with all peripherals running, and code fetched from code flash while modify operation ongoing on data flash. Notice that this value can be significantly reduced by application: switch off not used peripherals (default), reduce peripheral frequency through internal prescaler, fetch from RAM most used functions, use low power mode when possible.
- ³ Higher current may be sunk by device during power-up and standby exit. Please refer to in-rush average current in [Table 25](#).
- ⁴ RUN current measured with typical application with accesses on both Flash and RAM.
- ⁵ Only for the “P” classification: Data and Code Flash in Normal Power. Code fetched from RAM: Serial IPs CAN and LIN in loop back mode, DSPI as Master, PLL as system clock (4 x Multiplier) peripherals on (eMIOS/CTU/ADC) and running at max frequency, periodic SW/WDG timer reset enabled.
- ⁶ Data Flash Power Down. Code Flash in Low Power. SIRC 128 kHz and FIRC 16 MHz on. 10 MHz XTAL clock. FlexCAN: instances: 0, 1, 2 ON (clocked but not reception or transmission), instances: 4, 5, 6 clocks gated. LINFlex: instances: 0, 1, 2 ON (clocked but not reception or transmission), instance: 3 to 9 clocks gated. eMIOS: instance: 0 ON (16 channels on PA[0]–PA[11] and PC[12]–PC[15]) with PWM 20 kHz, instance: 1 clock gated. DSPI: instance: 0 (clocked but no communication), instance: 1 to 5 clocks gated. RTC/API ON. PIT ON. STM ON. ADC1 OFF. ADC0 ON but no conversion except two analog watchdogs.
- ⁷ Only for the “P” classification: No clock, FIRC 16 MHz off, SIRC 128 kHz on, PLL off, HPvreg off, ULPVreg/LPVreg on. All possible peripherals off and clock gated. Flash in power down mode.

4.9 Flash memory electrical characteristics

4.9.1 Program/erase characteristics

Table 28 shows the program and erase characteristics.

Table 28. Program and erase specifications

Symbol	C	Parameter	Conditions	Value				Unit
				Min	Typ ¹	Initial max ²	Max ³	
$t_{dwprogram}$	CC	Double word (64 bits) program time ⁴	Code Flash	—	18	50	500	μ s
			Data Flash		22			
$t_{16Kpperase}$		16 KB block preprogram and erase time	Code Flash	—	200	500	5000	ms
			Data Flash		300			
$t_{32Kpperase}$		32 KB block preprogram and erase time	Code Flash	—	300	600	5000	ms
			Data Flash		400			
$t_{128Kpperase}$		128 KB block preprogram and erase time	Code Flash	—	600	1300	7500	ms
			Data Flash		800			
t_{esus}		D	Erase Suspend Latency	—	—	30	30	μ s
t_{ESRT}		C	Erase Suspend Request Rate ⁵	Code Flash	20	—	—	—
	Data Flash			10	—	—	—	

¹ Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

² Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

³ The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

⁴ Actual hardware programming times. This does not include software overhead.

⁵ Time between erase suspend resume and the next erase suspend request

Table 29. Flash module life

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
P/E	CC	C	Number of program/erase cycles per block for 16 KB blocks over the operating temperature range (T _J)	—	100,000	—	—	cycles
P/E	CC	C	Number of program/erase cycles per block for 32 KB blocks over the operating temperature range (T _J)	—	10,000	100,000	—	cycles
P/E	CC	C	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T _J)	—	1,000	100,000	—	cycles
Retention	CC	C	Minimum data retention at 85 °C average ambient temperature ¹	Blocks with 0–1,000 P/E cycles	20	—	—	years
				Blocks with 1,001–10,000 P/E cycles	10	—	—	years
				Blocks with 10,001–100,000 P/E cycles	5	—	—	years

¹ Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 30. Flash read access timing

Symbol		C	Parameter	Conditions ¹	Max	Unit
f _{READ}	CC	P	Maximum frequency for Flash reading	2 wait states	64	MHz
		C		2 wait state	40	
		C		2 wait states	20	

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

4.9.2 Flash power supply DC characteristics

Table 31 shows the power supply DC characteristics on external supply.

Table 31. Flash power supply DC electrical characteristics

Symbol	Parameter	Conditions ¹	Value			Unit	
			Min	Typ	Max		
I _{CFREAD}	CC Sum of the current consumption on V _{DD_HV} and V _{DD_BV} on read access	Flash module read f _{CPU} = 64 MHz	Code Flash	—	—	33	mA
I _{DFREAD}			Data Flash	—	—	33	
I _{CFMOD}	CC Sum of the current consumption on V _{DD_HV} and V _{DD_BV} on matrix modification (program/erase)	Program/Erase on-going while reading Flash registers f _{CPU} = 64 MHz	Code Flash	—	—	52	mA
I _{DFMOD}			Data Flash	—	—	33	
I _{CFLPW}	CC Sum of the current consumption on V _{DD_HV} and V _{DD_BV} during Flash low power mode	—	Code Flash	—	—	1.1	mA
I _{DFLPW}			Data Flash	—	—	900	
I _{CFPWD}	CC Sum of the current consumption on V _{DD_HV} and V _{DD_BV} during Flash power down mode	—	Code Flash	—	—	150	μA
I _{DFPWD}			Data Flash	—	—	150	

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

4.9.3 Start-up/Switch-off timings

Table 32. Start-up time/Switch-off time

Symbol	C	Parameter	Conditions ¹	Value			Unit
				Min	Typ	Max	
t _{FLARSTEXIT}	CC	T Delay for Flash module to exit reset mode	—	—	—	125	μs
t _{FLALPEXIT}	CC	T Delay for Flash module to exit low-power mode	—	—	—	0.5	
t _{FLAPDEXIT}	CC	T Delay for Flash module to exit power-down mode	—	—	—	30	
t _{FLALPENTRY}	CC	T Delay for Flash module to enter low-power mode	—	—	—	0.5	
t _{FLAPDENTRY}	CC	T Delay for Flash module to enter power-down mode	—	—	—	1.5	

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

4.10 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

4.10.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and prequalification tests in relation with the EMC level requested for the application.

Electrical characteristics

- Software recommendations – The software flowchart must include the management of runaway conditions such as:
 - Corrupted program counter
 - Unexpected reset
 - Critical data corruption (control registers...)
- Prequalification trials – Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

4.10.2 Electromagnetic interference (EMI)

The product is monitored in terms of emission based on a typical application. This emission test conforms to the IEC61967-1 standard, which specifies the general conditions for EMI measurements.

Table 33. EMI radiated emission measurement^{1,2}

Symbol	C	Parameter	Conditions	Value			Unit		
				Min	Typ	Max			
—	SR	—	Scan range	—	0.150	—	1000	MHz	
f _{CPU}	SR	—	Operating frequency	—	64	—	—	MHz	
V _{DD_LV}	SR	—	LV operating voltages	—	1.28	—	—	V	
S _{EMI}	CC	T	Peak level	V _{DD} = 5 V, T _A = 25 °C, LQFP144 package Test conforming to IEC 61967-2, f _{OSC} = 8 MHz/f _{CPU} = 64 MHz	No PLL frequency modulation	—	—	18	dBμV
					± 2% PLL frequency modulation	—	—	14	dBμV

¹ EMI testing and I/O port waveforms per IEC 61967-1, -2, -4

² For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.

4.10.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

4.10.3.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

Table 34. ESD absolute maximum ratings^{1,2}

Symbol	Ratings	Conditions	Class	Max value ³	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	$T_A = 25\text{ °C}$ conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine Model)	$T_A = 25\text{ °C}$ conforming to AEC-Q100-003	M2	200	
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charged Device Model)	$T_A = 25\text{ °C}$ conforming to AEC-Q100-011	C3A	500 750 (corners)	

¹ All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

² A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

³ Data based on characterization results, not tested in production

4.10.3.2 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 35. Latch-up results

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	$T_A = 125\text{ °C}$ conforming to JESD 78	II level A

4.11 Fast external crystal oscillator (4 to 20 MHz) electrical characteristics

The device provides an oscillator/resonator driver. [Figure 11](#) describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

[Table 36](#) provides the parameter description of 4 MHz to 20 MHz crystals used for the design simulations.

Electrical characteristics

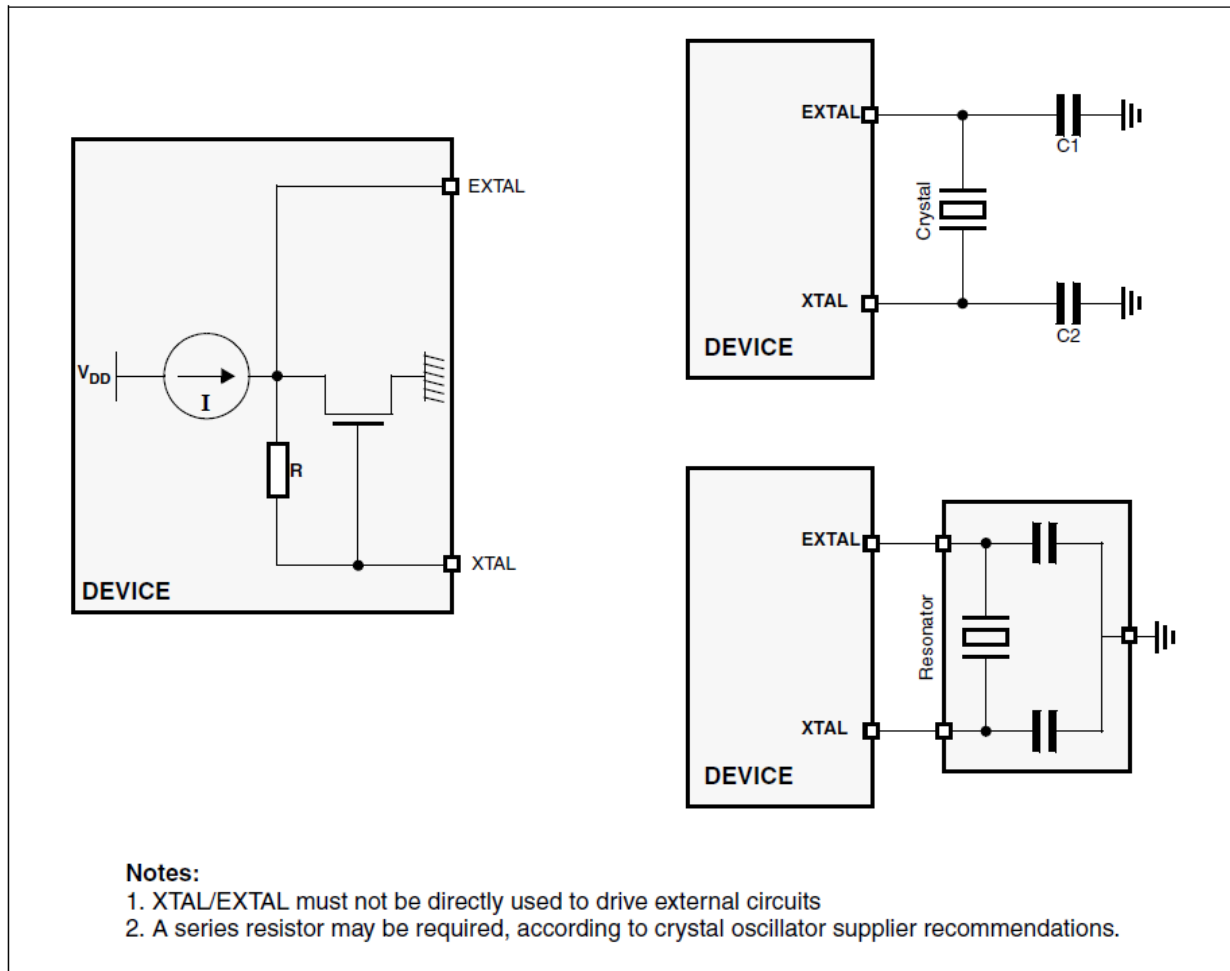


Figure 11. Crystal oscillator and resonator connection scheme

Table 36. Crystal description

Nominal frequency (MHz)	NDK crystal reference	Crystal equivalent series resistance ESR Ω	Crystal motional capacitance (C_m) fF	Crystal motional inductance (L_m) mH	Load on xtalin/xtalout $C1 = C2$ (pF) ¹	Shunt capacitance between xtalout and xtalin $C0^2$ (pF)
4	NX8045GB	300	2.68	591.0	21	2.93
8	NX5032GA	300	2.46	160.7	17	3.01
10		150	2.93	86.6	15	2.91
12		120	3.11	56.5	15	2.93
16		120	3.90	25.3	10	3.00

¹ The values specified for C1 and C2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.

² The value of C0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

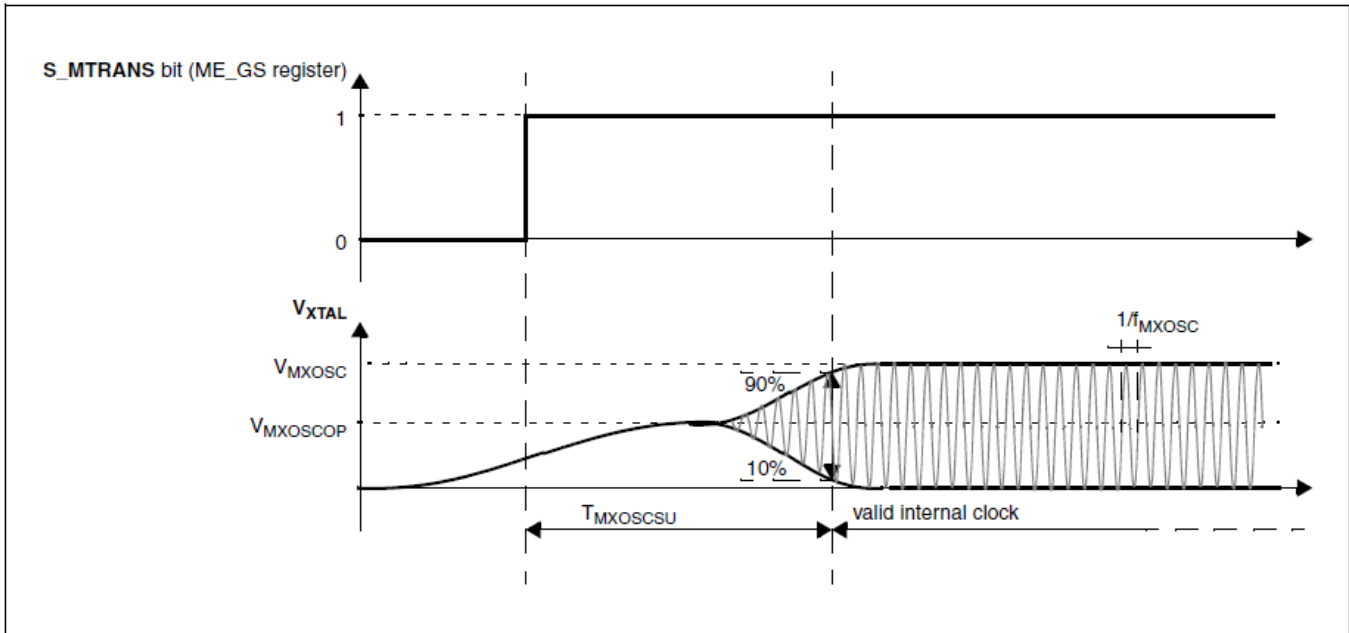


Figure 12. Fast external crystal oscillator (4 to 20 MHz) timing diagram

Table 37. Fast external crystal oscillator (4 to 20 MHz) electrical characteristics

Symbol	C	Parameter	Conditions ¹	Value			Unit	
				Min	Typ	Max		
f _{FXOSC}	SR	—	Fast external crystal oscillator frequency	4.0	—	20.0	MHz	
g _{mFXOSC}	CC	C	Fast external crystal oscillator transconductance	V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 0	2.2	—	8.2	mA/V
	CC	P		V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 0	2.0	—	7.4	
	CC	C		V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 1	2.7	—	9.7	
	CC	C		V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 1	2.5	—	9.2	
V _{FXOSC}	CC	T	Oscillation amplitude at EXTAL	f _{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0	1.3	—	—	V
				f _{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1	1.3	—	—	
V _{FXOSCOIP}	CC	C	Oscillation operating point	—	0.95	—	V	
I _{FXOSC} ²	CC	T	Fast external crystal oscillator consumption	—	2	3	mA	

Table 37. Fast external crystal oscillator (4 to 20 MHz) electrical characteristics (continued)

Symbol	C	Parameter	Conditions ¹	Value			Unit
				Min	Typ	Max	
t _{FXOSCSU}	CC	Fast external crystal oscillator start-up time	f _{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0	—	—	6	ms
			f _{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1	—	—	1.8	
V _{IH}	SR	Input high level CMOS (Schmitt Trigger)	Oscillator bypass mode	0.65V _{DD}	—	V _{DD} + 0.4	V
V _{IL}	SR	Input low level CMOS (Schmitt Trigger)	Oscillator bypass mode	-0.4	—	0.35V _{DD}	V

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

² Stated values take into account only analog module consumption but not the digital contributor (clock tree and enabled peripherals).

4.12 Slow external crystal oscillator (32 kHz) electrical characteristics

The device provides a low power oscillator/resonator driver.

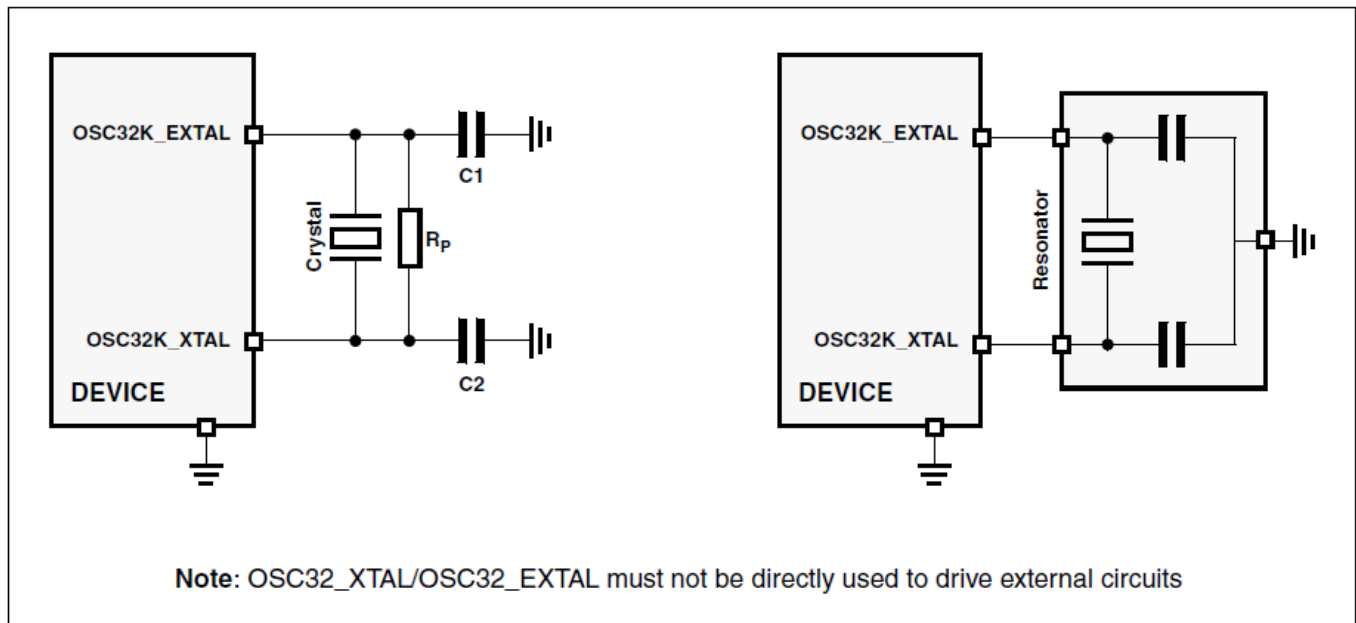


Figure 13. Crystal oscillator and resonator connection scheme

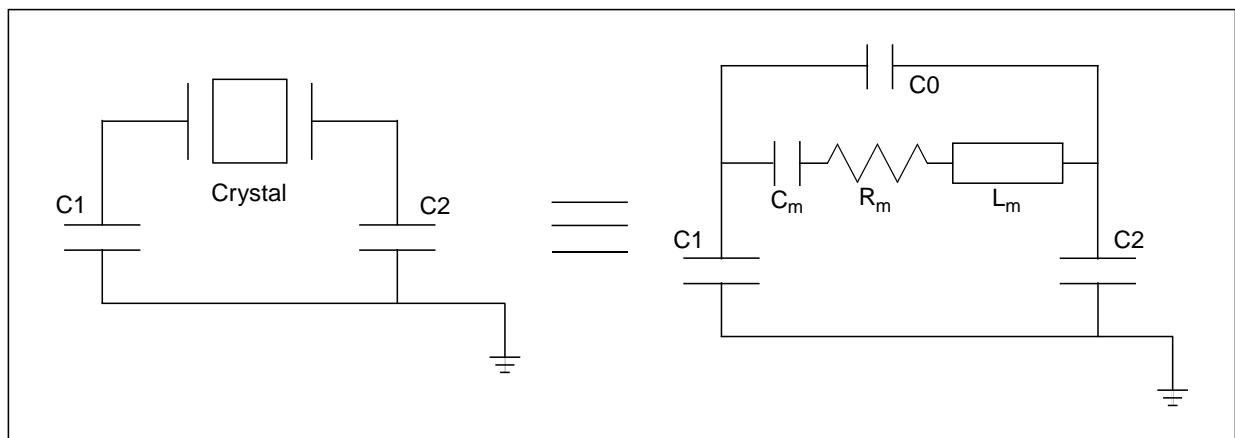


Figure 14. Equivalent circuit of a quartz crystal

Table 38. Crystal motional characteristics¹

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
L_m	Motional inductance	—	—	11.796	—	KH
C_m	Motional capacitance	—	—	2	—	fF
C1/C2	Load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground ²	—	18	—	28	pF
R_m ³	Motional resistance	AC coupled at $C_0 = 2.85 \text{ pF}$ ⁴	—	—	65	k Ω
		AC coupled at $C_0 = 4.9 \text{ pF}$ ⁴	—	—	50	
		AC coupled at $C_0 = 7.0 \text{ pF}$ ⁴	—	—	35	
		AC coupled at $C_0 = 9.0 \text{ pF}$ ⁴	—	—	30	

¹ The crystal used is Epson Toyocom MC306.

² This is the recommended range of load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground. It includes all the parasitics due to board traces, crystal and package.

³ Maximum ESR (R_m) of the crystal is 50 k Ω

⁴ C_0 Includes a parasitic capacitance of 2.0 pF between OSC32K_XTAL and OSC32K_EXTAL pins.

Electrical characteristics

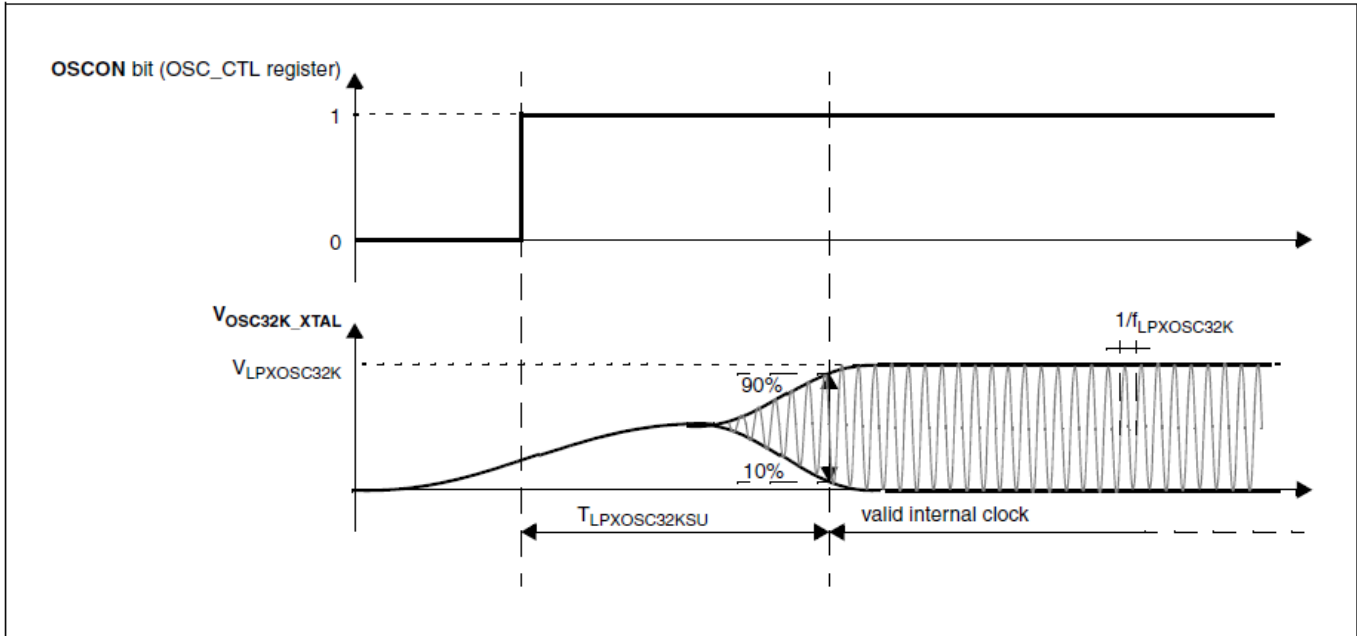


Figure 15. Slow external crystal oscillator (32 kHz) timing diagram

Table 39. Slow external crystal oscillator (32 kHz) electrical characteristics

Symbol	C	Parameter	Conditions ¹	Value			Unit
				Min	Typ	Max	
f_{SXOSC}	SR	—	Slow external crystal oscillator frequency	32	32.768	40	kHz
V_{SXOSC}	CC	T	Oscillation amplitude	—	2.1	—	V
$I_{SXOSCBIAS}$	CC	T	Oscillation bias current	—	2.5		μ A
I_{SXOSC}	CC	T	Slow external crystal oscillator consumption	—	—	8	μ A
$t_{SXOSCSU}$	CC	T	Slow external crystal oscillator start-up time	—	—	2 ²	s

¹ $V_{DD} = 3.3 \text{ V} \pm 10\% / 5.0 \text{ V} \pm 10\%$, $T_A = -40$ to $125 \text{ }^\circ\text{C}$, unless otherwise specified. Values are specified for no neighbor GPIO pin activity. If oscillator is enabled (OSC32K_XTAL and OSC32K_EXTAL pins), neighboring pins should not toggle.

² Start-up time has been measured with EPSON TOYOCOM MC306 crystal. Variation may be seen with other crystal.

4.13 FMPLL electrical characteristics

The device provides a frequency modulated phase locked loop (FMPLL) module to generate a fast system clock from the main oscillator driver.

Table 40. FMPLL electrical characteristics

Symbol	C	Parameter	Conditions ¹	Value			Unit	
				Min	Typ	Max		
f _{PLLIN}	SR	—	FMPLL reference clock ²	—	4	—	64	MHz

Electrical characteristics

Table 40. FMPLL electrical characteristics (continued)

Symbol	C	Parameter	Conditions ¹	Value			Unit	
				Min	Typ	Max		
Δ_{PLLIN}	SR	—	FMPLL reference clock duty cycle ²	40	—	60	%	
f_{PULO}	CC	P	FMPLL output clock frequency	16	—	64	MHz	
f_{VCO} ³	CC	P	VCO frequency without frequency modulation	256	—	512	MHz	
		P	VCO frequency with frequency modulation	245.76	—	532.48		
f_{CPU}	SR	—	System clock frequency	—	—	64	MHz	
f_{FREE}	CC	P	Free-running frequency	20	—	150	MHz	
t_{LOCK}	CC	P	FMPLL lock time	Stable oscillator ($f_{PLLIN} = 16$ MHz)		40	100	μ s
Δt_{STJIT}	CC	—	FMPLL short term jitter ⁴	f_{sys} maximum		−4	4	%
Δt_{LTJIT}	CC	—	FMPLL long term jitter	f_{PLLCLK} at 64 MHz, 4000 cycles		—	10	ns
I_{PLL}	CC	C	FMPLL consumption	$T_A = 25$ °C		—	4	mA

¹ $V_{DD} = 3.3$ V \pm 10% / 5.0 V \pm 10%, $T_A = -40$ to 125 °C, unless otherwise specified

² PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN} .

³ Frequency modulation is considered \pm 4%.

⁴ Short term jitter is measured on the clock rising edge at cycle n and n+4.

4.14 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz main internal RC oscillator. This is used as the default clock at the power-up of the device.

Table 41. Fast internal RC oscillator (16 MHz) electrical characteristics

Symbol	C	Parameter	Conditions ¹	Value			Unit		
				Min	Typ	Max			
f_{FIRC}	CC	P	Fast internal RC oscillator high frequency	$T_A = 25$ °C, trimmed		—	16	MHz	
	SR	—		—	12	—	20		
I_{FIRCUN} ²	CC	T	Fast internal RC oscillator high frequency current in running mode	$T_A = 25$ °C, trimmed		—	—	200	μ A
$I_{FIRCPWD}$	CC	D	Fast internal RC oscillator high frequency current in power down mode	$T_A = 25$ °C		—	—	10	μ A

Table 41. Fast internal RC oscillator (16 MHz) electrical characteristics (continued)

Symbol	C	Parameter	Conditions ¹	Value			Unit		
				Min	Typ	Max			
I _{FIRCSTOP}	CC	T	Fast internal RC oscillator high frequency and system clock current in stop mode	T _A = 25 °C	sysclk = off	—	500	—	μA
					sysclk = 2 MHz	—	600	—	
					sysclk = 4 MHz	—	700	—	
					sysclk = 8 MHz	—	900	—	
					sysclk = 16 MHz	—	1250	—	
t _{FIRCSU}	CC	C	Fast internal RC oscillator start-up time	V _{DD} = 5.0 V ± 10%	—	1.1	2.0	μs	
Δ _{FIRCPRE}	CC	C	Fast internal RC oscillator precision after software trimming of f _{FIRC}	T _A = 25 °C	-1	—	1	%	
Δ _{FIRCTRIM}	CC	C	Fast internal RC oscillator trimming step	T _A = 25 °C	—	1.6	—	%	
Δ _{FIRCVAR}	CC	C	Fast internal RC oscillator variation over temperature and supply with respect to f _{FIRC} at T _A = 25 °C in high-frequency configuration	—	-5	—	5	%	

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

4.15 Slow internal RC oscillator (128 kHz) electrical characteristics

The device provides a 128 kHz low power internal RC oscillator. This can be used as the reference clock for the RTC module.

Table 42. Slow internal RC oscillator (128 kHz) electrical characteristics

Symbol	C	Parameter	Conditions ¹	Value			Unit	
				Min	Typ	Max		
f _{SIRC}	CC	P	Slow internal RC oscillator low frequency	T _A = 25 °C, trimmed	—	128	—	kHz
	SR				—	100	—	
I _{SIRC} ^{2,}	CC	C	Slow internal RC oscillator low frequency current	T _A = 25 °C, trimmed	—	—	5	μA
t _{SIRCSU}	CC	P	Slow internal RC oscillator start-up time	T _A = 25 °C, V _{DD} = 5.0 V ± 10%	—	8	12	μs
Δ _{SIRCPRE}	CC	C	Slow internal RC oscillator precision after software trimming of f _{SIRC}	T _A = 25 °C	-2	—	2	%
Δ _{SIRCTRIM}	CC	C	Slow internal RC oscillator trimming step	—	—	2.7	—	

Table 42. Slow internal RC oscillator (128 kHz) electrical characteristics (continued)

Symbol	C	Parameter	Conditions ¹	Value			Unit	
				Min	Typ	Max		
Δ_{SIRCVAR}	CC	C	Slow internal RC oscillator variation in temperature and supply with respect to f_{SIRC} at $T_A = 55\text{ °C}$ in high frequency configuration	High frequency configuration	-10	—	10	%

¹ $V_{\text{DD}} = 3.3\text{ V} \pm 10\% / 5.0\text{ V} \pm 10\%$, $T_A = -40\text{ to }125\text{ °C}$, unless otherwise specified

² This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

4.16 ADC electrical characteristics

4.16.1 Introduction

The device provides two Successive Approximation Register (SAR) analog-to-digital converters (10-bit and 12-bit).

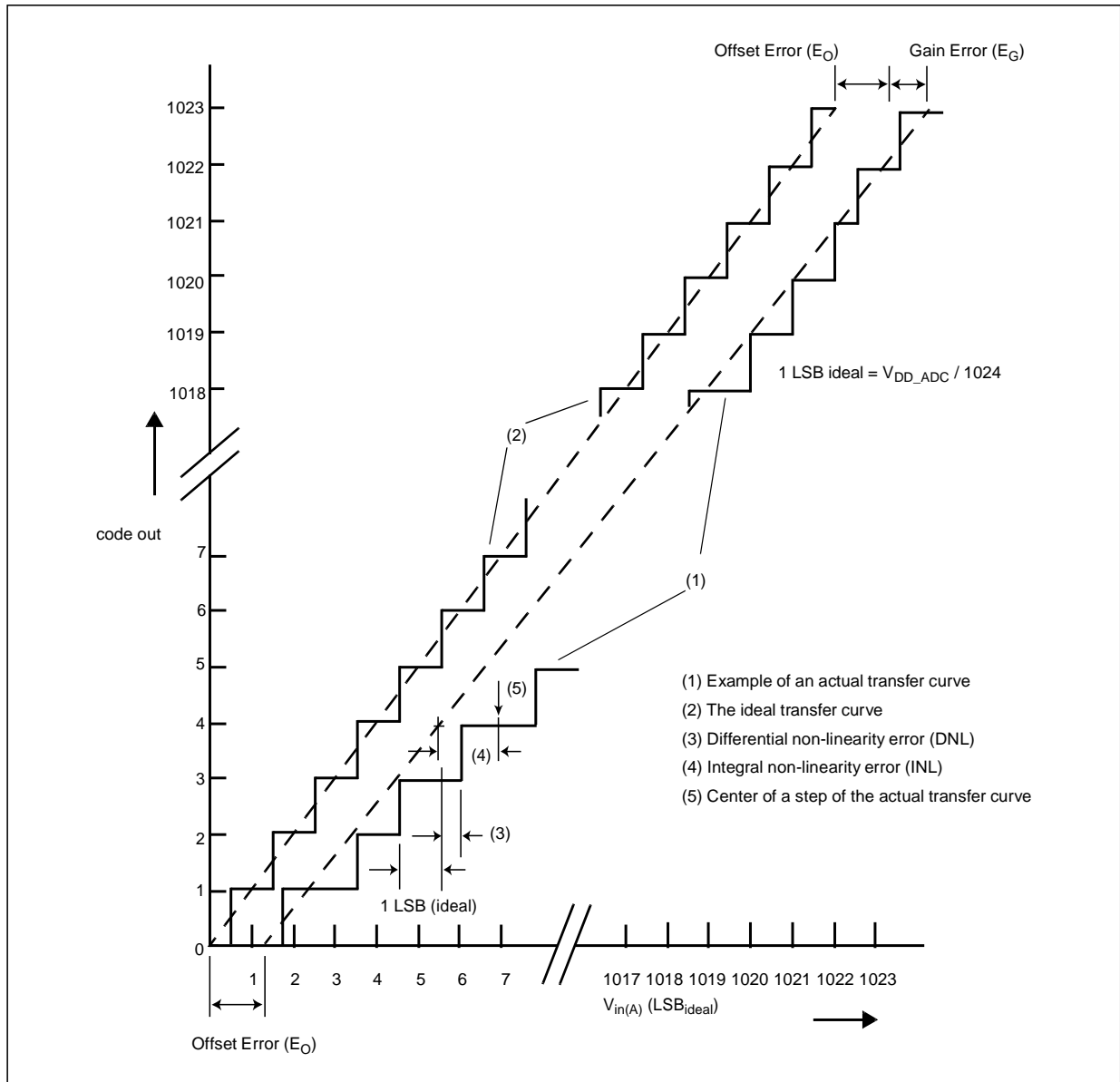


Figure 16. ADC_0 characteristic and error definitions

4.16.2 Input impedance and ADC accuracy

In the following analysis, the input circuit corresponding to the precise channels is considered.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer

Electrical characteristics

or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: being C_S and C_{p2} substantially two switched capacitances, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with $C_S + C_{p2}$ equal to 3 pF, a resistance of 330 k Ω is obtained ($R_{EQ} = 1 / (f_c \times (C_S + C_{p2}))$), where f_c represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on $C_S + C_{p2}$) and the sum of $R_S + R_F$, the external circuit must be designed to respect the [Equation 4](#):

Eqn. 4

$$V_A \cdot \frac{R_S + R_F}{R} < \frac{1}{2} \text{ SB}$$

EQ

[Equation 4](#) generates a constraint for external network design, in particular on a resistive path.

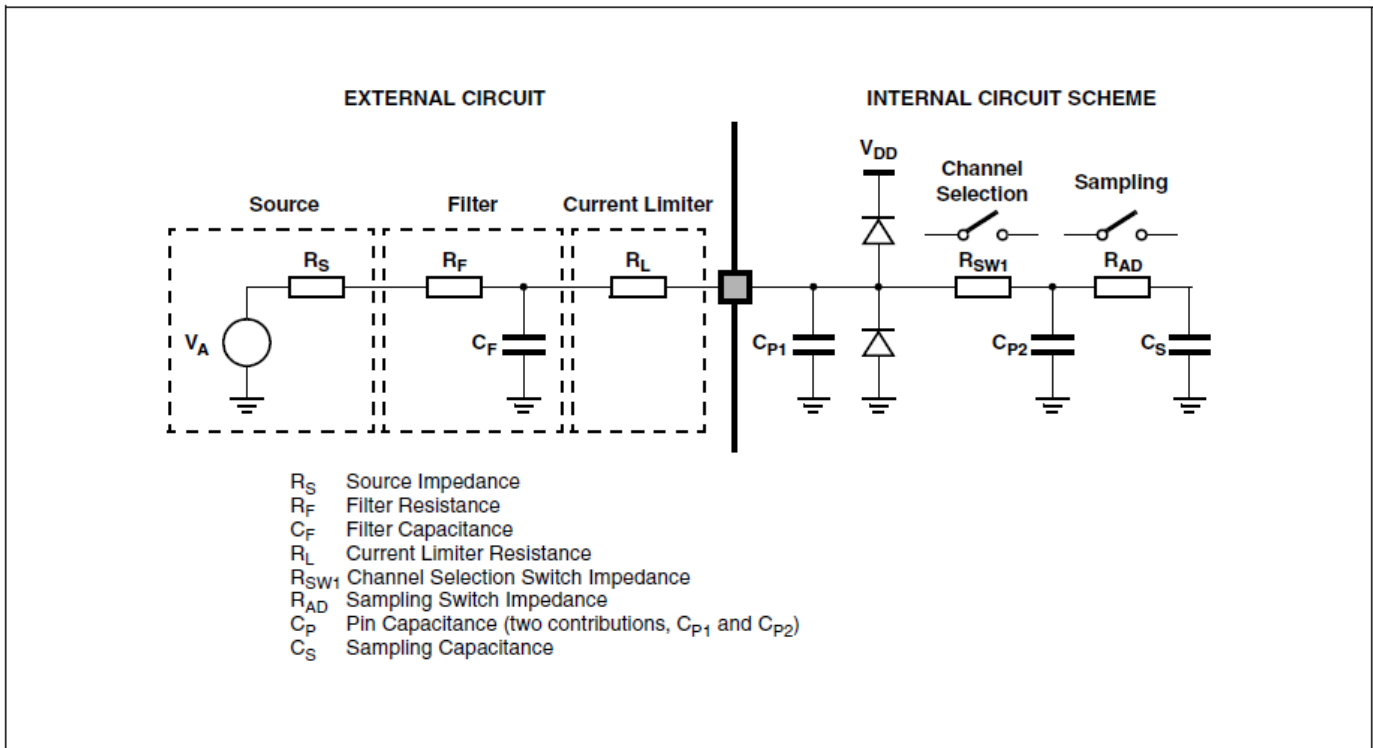


Figure 17. Input equivalent circuit (precise channels)

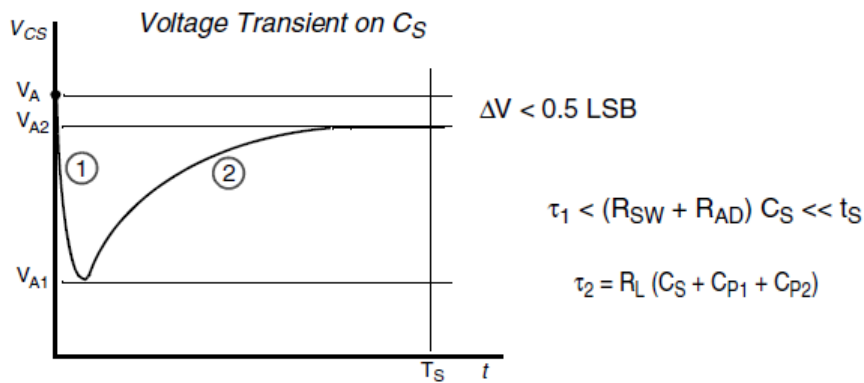


Figure 18. Input equivalent circuit (extended channels)

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F , C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in [Figure 17](#)): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

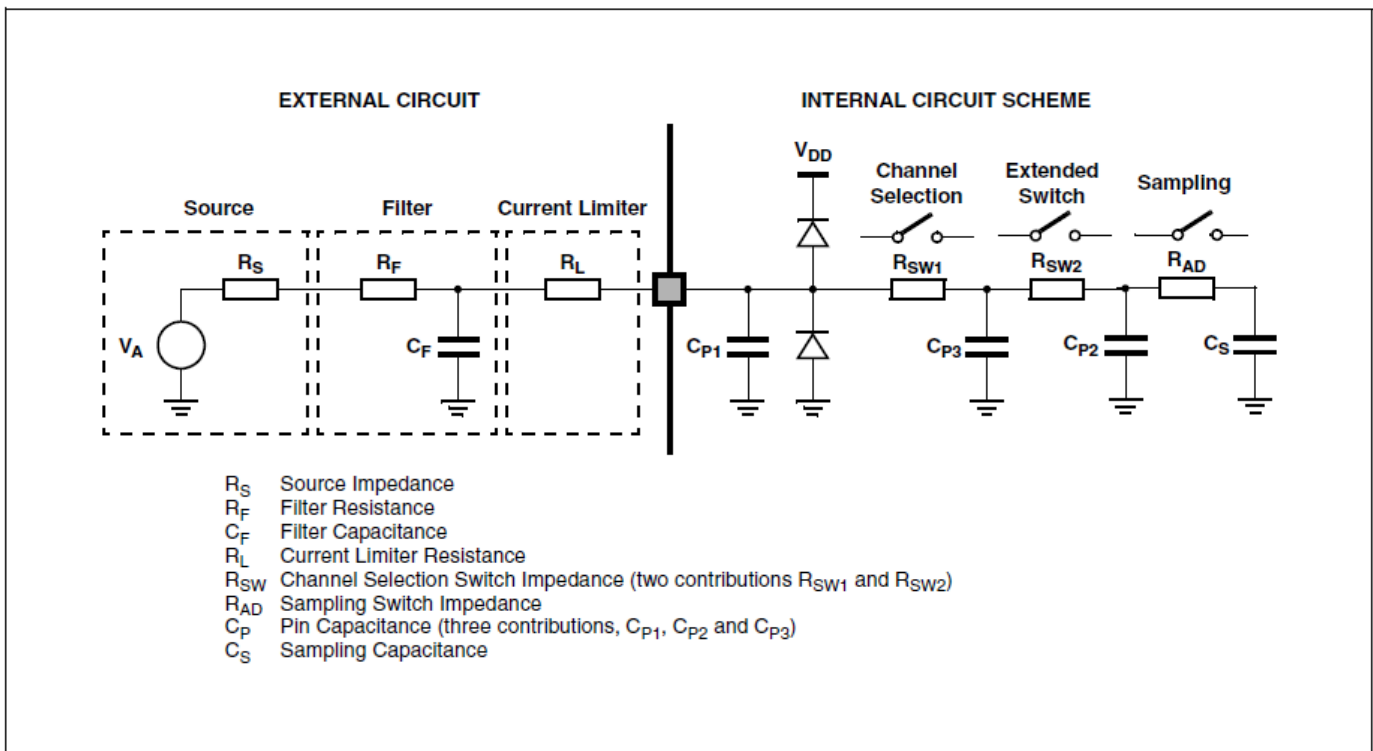


Figure 19. Transient behavior during sampling phase

Electrical characteristics

In particular two different transient periods can be distinguished:

1. A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Eqn. 5

$$\tau_1 = (R_{SW} + R_{AD}) \cdot \frac{C_P \cdot C_S}{C_P + C_S}$$

[Equation 5](#) can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time t_s is always much longer than the internal time constant:

Eqn. 6

$$\tau_1 < (R_{SW} + R_{AD}) \cdot C_S \ll t_s$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S , determining a new value of the voltage V_{A1} on the capacitance according to [Equation 7](#):

Eqn. 7

$$V_{A1} \cdot (C_S + C_{P1} + C_{P2}) = V_A \cdot (C_{P1} + C_{P2})$$

2. A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L : again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Eqn. 8

$$\tau_2 < R_L \cdot (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time t_s , a constraints on R_L sizing is obtained:

ADC_0 (10-bit)**Eqn. 9**

$$8.5 \cdot \tau_2 = 8.5 \cdot R_L \cdot (C_S + C_{P1} + C_{P2}) < t_s$$

ADC_1 (12-bit)**Eqn. 10**

$$10 \cdot \tau_2 = 10 \cdot R_L \cdot (C_S + C_{P1} + C_{P2}) < t_s$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1} , C_{P2} and C_S , then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1} . Equation 11 must be respected (charge balance assuming now C_S already charged at V_{A1}):

Eqn. 11

$$V_{A2} \cdot (C_S + C_{P1} + C_{P2} + C_F) = V_A \cdot C_F + V_{A1} \cdot (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A ; the time constant $R_F C_F$ of the filter is very high with respect to the sampling time (t_s). The filter is typically designed to act as antialiasing.

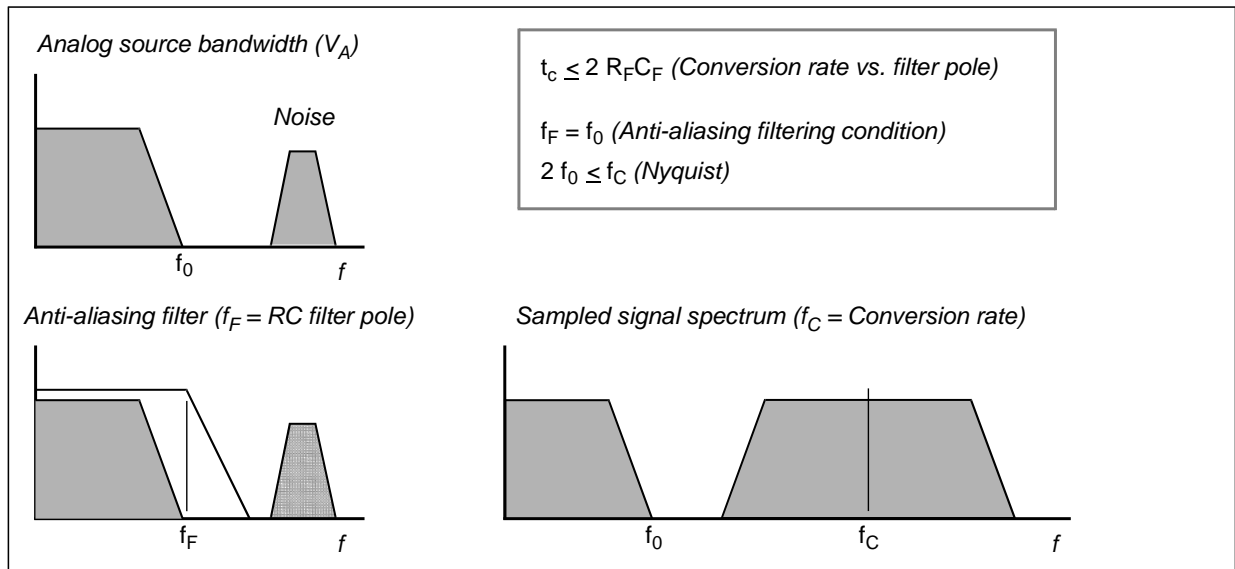


Figure 20. Spectral representation of input signal

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the antialiasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (t_c). Again the conversion period t_c is longer than the sampling time t_s , which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in

Electrical characteristics

conclusion it is evident that the time constant of the filter $R_F C_F$ is definitively much higher than the sampling time t_s , so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S ; from the two charge balance equations above, it is simple to derive [Equation 12](#) between the ideal and real sampled voltage on C_S :

Eqn. 12

$$\frac{V_{A2}}{V_A} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

ADC_0 (10-bit)

Eqn. 13

$$C_F > 2048 \cdot C_S$$

ADC_1 (12-bit)

Eqn. 14

$$C_F > 8192 \cdot C_S$$

4.16.3 ADC electrical characteristics

Table 43. ADC input leakage current

Symbol	C	Parameter	Conditions	Value			Unit		
				Min	Typ	Max			
I _{LKG}	CC	D	Input leakage current	T _A = -40 °C	No current injection on adjacent pin	—	1	70	nA
				T _A = 25 °C		—	1	70	
				T _A = 85 °C		—	3	100	
				T _A = 105 °C		—	8	200	
				T _A = 125 °C		—	45	400	

Table 44. ADC_0 conversion characteristics (10-bit ADC_0)

Symbol	C	Parameter	Conditions ¹	Value			Unit
				Min	Typ	Max	
V _{SS_ADC0}	SR	—	Voltage on VSS_HV_ADC0 (ADC_0 reference) pin with respect to ground (V _{SS}) ²	—	—	0.1	V
V _{DD_ADC0}	SR	—	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V _{SS})	—	—	V _{DD} + 0.1	V
V _{AINx}	SR	—	Analog input voltage ³	—	—	V _{DD_ADC0} + 0.1	V
I _{ADC0pwd}	SR	—	ADC_0 consumption in power down mode	—	—	50	μA
I _{ADC0run}	SR	—	ADC_0 consumption in running mode	—	—	5	mA
f _{ADC0}	SR	—	ADC_0 analog frequency	—	—	32 + 4%	MHz
Δ _{ADC0_SYS}	SR	—	ADC_0 digital clock duty cycle (ipg_clk)	ADCLKSEL = 1 ⁴	—	55	%
t _{ADC0_PU}	SR	—	ADC_0 power up delay	—	—	1.5	μs
t _{ADC0_S}	CC	T	Sampling time ⁵	f _{ADC} = 32 MHz, INPSAMP = 17	—	—	μs
				f _{ADC} = 6 MHz, INPSAMP = 255	—	—	

Electrical characteristics

Table 44. ADC_0 conversion characteristics (10-bit ADC_0) (continued)

Symbol	C	Parameter	Conditions ¹	Value			Unit		
				Min	Typ	Max			
t _{ADC0_C}	CC	P	Conversion time ⁶	f _{ADC} = 32 MHz, INPCMP = 2	0.625	—	—	μs	
C _S	CC	D	ADC_0 input sampling capacitance	—	—	—	3	pF	
C _{P1}	CC	D	ADC_0 input pin capacitance 1	—	—	—	3	pF	
C _{P2}	CC	D	ADC_0 input pin capacitance 2	—	—	—	1	pF	
C _{P3}	CC	D	ADC_0 input pin capacitance 3	—	—	—	1	pF	
R _{SW1}	CC	D	Internal resistance of analog source	—	—	—	3	kΩ	
R _{SW2}	CC	D	Internal resistance of analog source	—	—	—	2	kΩ	
R _{AD}	CC	D	Internal resistance of analog source	—	—	—	2	kΩ	
I _{INJ}	SR	—	Input current Injection	Current injection on one ADC_0 input, different from the converted one	V _{DD} = 3.3 V ± 10%	-5	—	5	mA
					V _{DD} = 5.0 V ± 10%	-5	—	5	
INL	CC	T	Absolute integral nonlinearity	No overload	—	0.5	1.5	LSB	
DNL	CC	T	Absolute differential nonlinearity	No overload	—	0.5	1.0	LSB	
E _O	CC	T	Absolute offset error	—	—	0.5	—	LSB	
E _G	CC	T	Absolute gain error	—	—	0.6	—	LSB	
TUEP	CC	P	Total unadjusted error ⁷ for precise channels, input only pins	Without current injection	-2	0.6	2	LSB	
		T		With current injection	-3	—	3		
TUEX	CC	T	Total unadjusted error ⁷ for extended channel	Without current injection	-3	1	3	LSB	
		T		With current injection	-4	—	4		

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

² Analog and digital V_{SS} **must** be common (to be tied together externally).

³ V_{AINx} may exceed V_{SS_ADC0} and V_{DD_ADC0} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.

⁴ Duty cycle is ensured by using system clock without prescaling. When ADCLKSEL = 0, the duty cycle is ensured by internal divider by 2.

⁵ During the sampling time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC0_S}. After the end of the sampling time t_{ADC0_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sampling clock t_{ADC0_S} depend on programming.

⁶ This parameter does not include the sampling time t_{ADC0_S}, but only the time for determining the digital result and the time to load the result's register with the conversion result.

⁷ Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

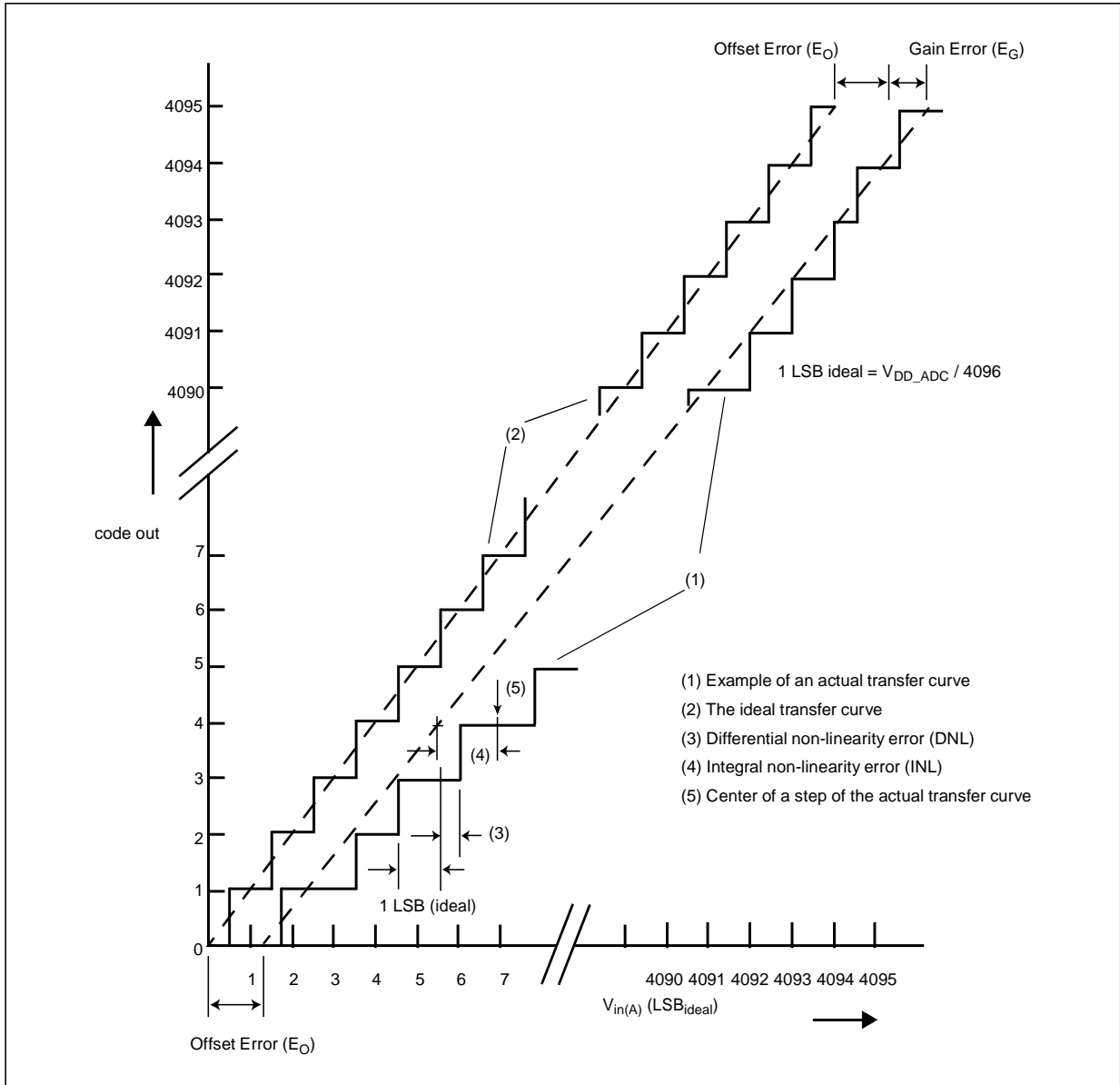


Figure 21. ADC_1 characteristic and error definitions

Table 45. ADC_1 conversion characteristics (12-bit ADC_1)

Symbol	C	Parameter	Conditions ¹	Value			Unit
				Min	Typ	Max	
V _{SS_ADC1}	SR	—	—	-0.1	—	0.1	V
V _{DD_ADC1}	SR	—	—	V _{DD} - 0.1	—	V _{DD} + 0.1	V

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Table 45. ADC_1 conversion characteristics (12-bit ADC_1) (continued)

Symbol	C	Parameter	Conditions ¹	Value			Unit	
				Min	Typ	Max		
V _{AINx}	SR	—	Analog input voltage ³	—	—	—	V	
I _{ADC1pwd}	SR	—	ADC_1 consumption in power down mode	—	—	50	μA	
I _{ADC1run}	SR	—	ADC_1 consumption in running mode	—	—	6	mA	
f _{ADC1}	SR	—	ADC_1 analog frequency	V _{DD} = 3.3 V	3.33	—	20 + 4%	MHz
				V _{DD} = 5 V	3.33	—	32 + 4%	
t _{ADC1_PU}	SR	—	ADC_1 power up delay	—	—	1.5	μs	
t _{ADC1_S}	CC	T	Sampling time ⁴ V _{DD} = 3.3 V	f _{ADC1} = 20 MHz, INPSAMP = 12	600	—	—	ns
			Sampling time ⁴ V _{DD} = 5.0 V	f _{ADC1} = 32 MHz, INPSAMP = 17	500	—	—	
			Sampling time ⁴ V _{DD} = 3.3 V	f _{ADC1} = 3.33 MHz, INPSAMP = 255	—	—	76.2	μs
			Sampling time ⁴ V _{DD} = 5.0 V	f _{ADC1} = 3.33 MHz, INPSAMP = 255	—	—	76.2	
t _{ADC1_C}	CC	P	Conversion time ⁵ V _{DD} = 3.3 V	f _{ADC1} = 20 MHz, INPCMP = 0	2.4	—	—	μs
			Conversion time ⁵ V _{DD} = 5.0 V	f _{ADC1} = 32 MHz, INPCMP = 0	1.5	—	—	μs
			Conversion time ⁵ V _{DD} = 3.3 V	f _{ADC1} = 13.33 MHz, INPCMP = 0	—	—	3.6	μs
			Conversion time ⁵ V _{DD} = 5.0 V	f _{ADC1} = 13.33 MHz, INPCMP = 0	—	—	3.6	μs
Δ _{ADC1_SYS}	SR	—	ADC_1 digital clock duty cycle	ADCLKSEL = 1 ⁶	45	—	55	%
C _S	CC	D	ADC_1 input sampling capacitance	—	—	—	5	pF
C _{P1}	CC	D	ADC_1 input pin capacitance 1	—	—	—	3	pF
C _{P2}	CC	D	ADC_1 input pin capacitance 2	—	—	—	1	pF
C _{P3}	CC	D	ADC_1 input pin capacitance 3	—	—	—	1.5	pF
R _{SW1}	CC	D	Internal resistance of analog source	—	—	—	1	kΩ
R _{SW2}	CC	D	Internal resistance of analog source	—	—	—	2	kΩ
R _{AD}	CC	D	Internal resistance of analog source	—	—	—	0.3	kΩ

Table 45. ADC_1 conversion characteristics (12-bit ADC_1) (continued)

Symbol	C	Parameter	Conditions ¹		Value			Unit	
					Min	Typ	Max		
I _{INJ}	SR	—	Input current Injection	Current injection on one ADC_1 input, different from the converted one	V _{DD} = 3.3 V ± 10%	−5	—	5	mA
					V _{DD} = 5.0 V ± 10%	−5	—	5	
INLP	CC	T	Absolute integral nonlinearity – Precise channels	No overload		—	1	3	LSB
INLX	CC	T	Absolute integral nonlinearity – Extended channels	No overload		—	1.5	5	LSB
DNL	CC	T	Absolute differential nonlinearity	No overload		—	0.5	1	LSB
E _O	CC	T	Absolute offset error	—		—	2	—	LSB
E _G	CC	T	Absolute gain error	—		—	2	—	LSB
TUEP ⁷	CC	P	Total unadjusted error for precise channels, input only pins	Without current injection		−6	—	6	LSB
		T		With current injection		−8	—	8	
TUEX ⁷	CC	T	Total unadjusted error for extended channel	Without current injection		−10	—	10	LSB
		T		With current injection		−12	—	12	

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified

² Analog and digital V_{SS} **must** be common (to be tied together externally).

³ V_{AINx} may exceed V_{SS_ADC1} and V_{DD_ADC1} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0xFFF.

⁴ During the sampling time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC1_S}. After the end of the sampling time t_{ADC1_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sampling clock t_{ADC1_S} depend on programming.

⁵ This parameter does not include the sampling time t_{ADC1_S}, but only the time for determining the digital result and the time to load the result's register with the conversion result.

⁶ Duty cycle is ensured by using system clock without prescaling. When ADCLKSEL = 0, the duty cycle is ensured by internal divider by 2.

⁷ Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

4.17 On-chip peripherals

4.17.1 Current consumption

Table 46. On-chip peripherals current consumption¹

Symbol	C	Parameter	Conditions		Typical value ²	Unit	
I _{DD_BV(CAN)}	CC	T	CAN (FlexCAN) supply current on V _{DD_BV}	Bitrate: 500 Kbyte/s	Total (static + dynamic) consumption: • FlexCAN in loop-back mode • XTAL at 8 MHz used as CAN engine clock source • Message sending period is 580 μs	8 * f _{periph} + 85	μA
				Bitrate: 125 Kbyte/s		8 * f _{periph} + 27	
I _{DD_BV(eMIOS)}	CC	T	eMIOS supply current on V _{DD_BV}	Static consumption: • eMIOS channel OFF • Global prescaler enabled		29 * f _{periph}	μA
				Dynamic consumption: • It does not change varying the frequency (0.003 mA)		3	
I _{DD_BV(SCI)}	CC	T	SCI (LINFlex) supply current on V _{DD_BV}	Total (static + dynamic) consumption: • LIN mode • Baudrate: 20 Kbyte/s		5 * f _{periph} + 31	μA
I _{DD_BV(SPI)}	CC	T	SPI (DSPI) supply current on V _{DD_BV}	Ballast static consumption (only clocked)		1	μA
				Ballast dynamic consumption (continuous communication): • Baudrate: 2 Mbit/s • Transmission every 8 μs • Frame: 16 bits		16 * f _{periph}	
I _{DD_BV} (ADC_0/ADC_1)	CC	T	ADC_0/ADC_1 supply current on V _{DD_BV}	V _{DD} = 5.5 V	Ballast static consumption (no conversion) ³	41 * f _{periph}	μA
					Ballast dynamic consumption (continuous conversion) ³	46 * f _{periph}	
I _{DD_HV_ADC0}	CC	T	ADC_0 supply current on V _{DD_HV_ADC0}	V _{DD} = 5.5 V	Analog static consumption (no conversion)	200	μA
					Analog dynamic consumption (continuous conversion)	3	mA
I _{DD_HV_ADC1}	CC	T	ADC_1 supply current on V _{DD_HV_ADC1}	V _{DD} = 5.5 V	Analog static consumption (no conversion)	300 * f _{periph}	μA
					Analog dynamic consumption (continuous conversion)	4	mA
I _{DD_HV(FLASH)}	CC	T	CFlash + DFlash supply current on V _{DD_HV}	V _{DD} = 5.5 V	—	12	mA
I _{DD_HV(PLL)}	CC	T	PLL supply current on V _{DD_HV}	V _{DD} = 5.5 V	—	30 * f _{periph}	μA

- 1 Operating conditions: $T_A = 25^\circ\text{C}$, $f_{\text{periph}} = 8 \text{ MHz to } 64 \text{ MHz}$
- 2 f_{periph} is an absolute value.
- 3 During the conversion the total current consumption is given from the sum of the static and dynamic consumption
i.e. $(41 + 46) * f_{\text{periph}}$

4.17.2 DSPI characteristics

Table 47. DSPI characteristics¹

No.	Symbol	C	D	Parameter	DSPI0/DSPI1/DSPI3/DSPI5			DSPI2/DSPI4			Unit	
					Min	Typ	Max	Min	Typ	Max		
1	t_{SCK}	SR	D	SCK cycle time	Master mode (MTFE = 0)	125	—	—	333	—	—	ns
			D		Slave mode (MTFE = 0)	125	—	—	333	—	—	
			D		Master mode (MTFE = 1)	83	—	—	125	—	—	
			D		Slave mode (MTFE = 1)	83	—	—	125	—	—	
—	f_{DSPI}	SR	D	DSPI digital controller frequency	—	—	f_{CPU}	—	—	f_{CPU}	MHz	
—	Δt_{CSC}	CC	D	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->0	Master mode	—	—	130^2	—	—	15^3	ns
—	Δt_{ASC}	CC	D	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->1	Master mode	—	—	130^3	—	—	130^3	ns
2	$t_{CSCe_{xt}}^4$	SR	D	CS to SCK delay	Slave mode	32	—	—	32	—	—	ns
3	t_{ASCext}^5	SR	D	After SCK delay	Slave mode	$1/f_{DSPI} + 5$	—	—	$1/f_{DSPI} + 5$	—	—	ns
4	t_{SDC}	CC	D	SCK duty cycle	Master mode	—	$t_{SCK}/2$	—	—	$t_{SCK}/2$	—	ns
			D		Slave mode	$t_{SCK}/2$	—	—	$t_{SCK}/2$	—	—	
5	t_A	SR	D	Slave access time	Slave mode	—	—	$1/f_{DSPI} + 70$	—	—	$1/f_{DSPI} + 130$	ns
6	t_{DI}	SR	D	Slave SOUT disable time	Slave mode	7	—	—	7	—	—	ns
7	t_{PCSC}	SR	D	PCSx to PCSS time	—	0	—	—	0	—	—	ns
8	t_{PASC}	SR	D	PCSS to PCSx time	—	0	—	—	0	—	—	ns
9	t_{SUI}	SR	D	Data setup time for inputs	Master mode	43	—	—	145	—	—	ns
					Slave mode	5	—	—	5	—	—	

Table 47. DSPI characteristics¹ (continued)

No.	Symbol	C	Parameter	DSPI0/DSPI1/DSPI3/DSPI5			DSPI2/DSPI4			Unit		
				Min	Typ	Max	Min	Typ	Max			
10	t _{HI}	SR	D	Data hold time for inputs	Master mode	0	—	—	0	—	—	ns
					Slave mode	2 ⁶	—	—	2 ⁶	—	—	
11	t _{SUO} ⁷	CC	D	Data valid after SCK edge	Master mode	—	—	32	—	—	50	ns
					Slave mode	—	—	52	—	—	160	
12	t _{HO} ⁷	CC	D	Data hold time for outputs	Master mode	0	—	—	0	—	—	ns
					Slave mode	8	—	—	13	—	—	

¹ Operating conditions: C_L = 10 to 50 pF, Slew_{IN} = 3.5 to 15 ns

² Maximum value is reached when CSn pad is configured as SLOW pad while SCK pad is configured as MEDIUM. A positive value means that SCK starts before CSn is asserted. DSPI2 has only SLOW SCK available.

³ Maximum value is reached when CSn pad is configured as MEDIUM pad while SCK pad is configured as SLOW. A positive value means that CSn is deasserted before SCK. DSPI0 and DSPI1 have only MEDIUM SCK available.

⁴ The t_{CSC} delay value is configurable through a register. When configuring t_{CSC} (using PCSSCK and CSSCK fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{CSC} to ensure positive t_{CSCext}.

⁵ The t_{ASC} delay value is configurable through a register. When configuring t_{ASC} (using PASC and ASC fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{ASC} to ensure positive t_{ASCext}.

⁶ This delay value corresponds to SMPL_PT = 00b which is bit field 9 and 8 of DSPI_MCR register.

⁷ SCK and SOUT are configured as MEDIUM pad.

Figure 22. DSPI classic SPI timing — master, CPHA = 0

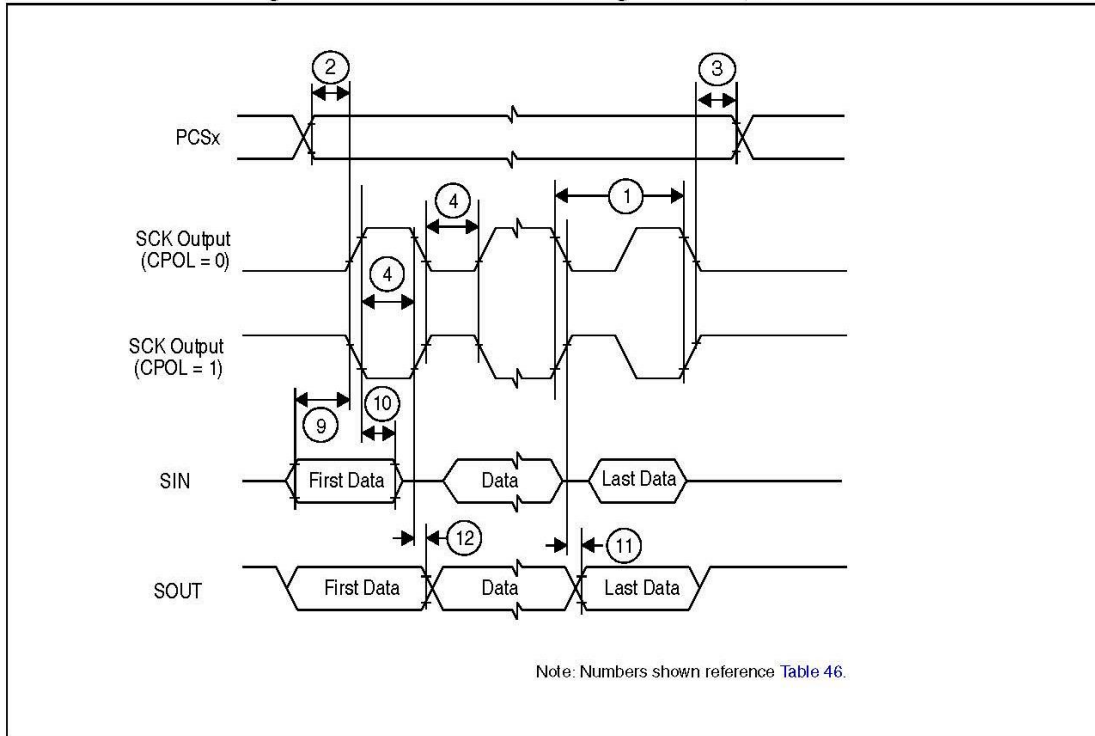


Figure 23. DSPI classic SPI timing — master, CPHA = 1

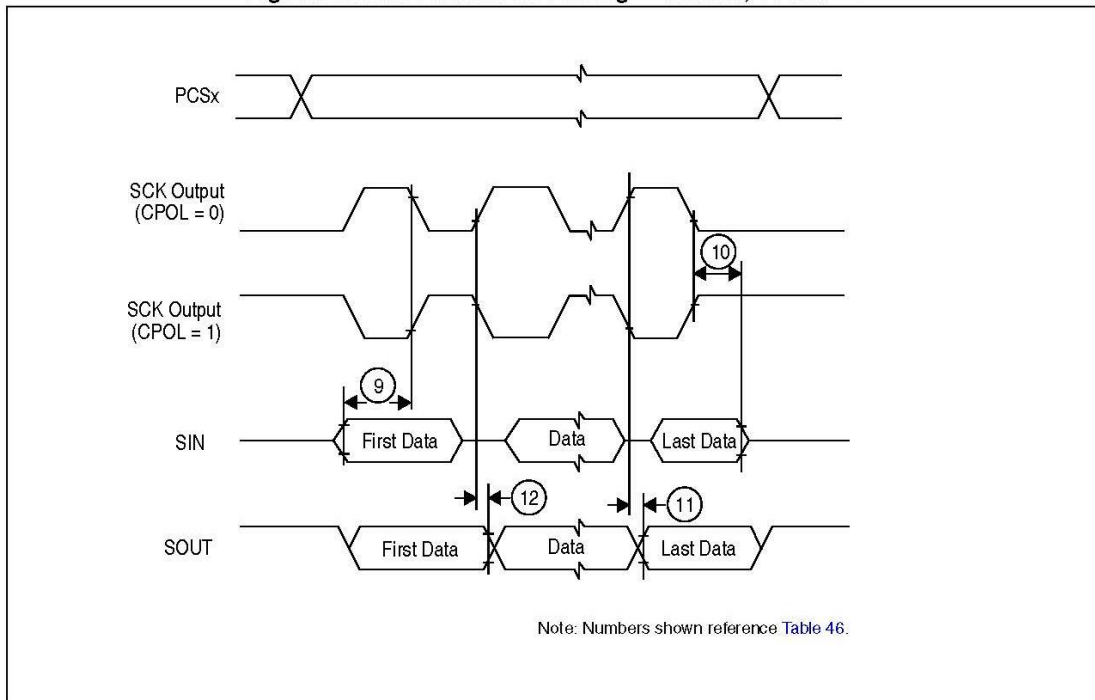


Figure 24. DSPI classic SPI timing — slave, CPHA = 0

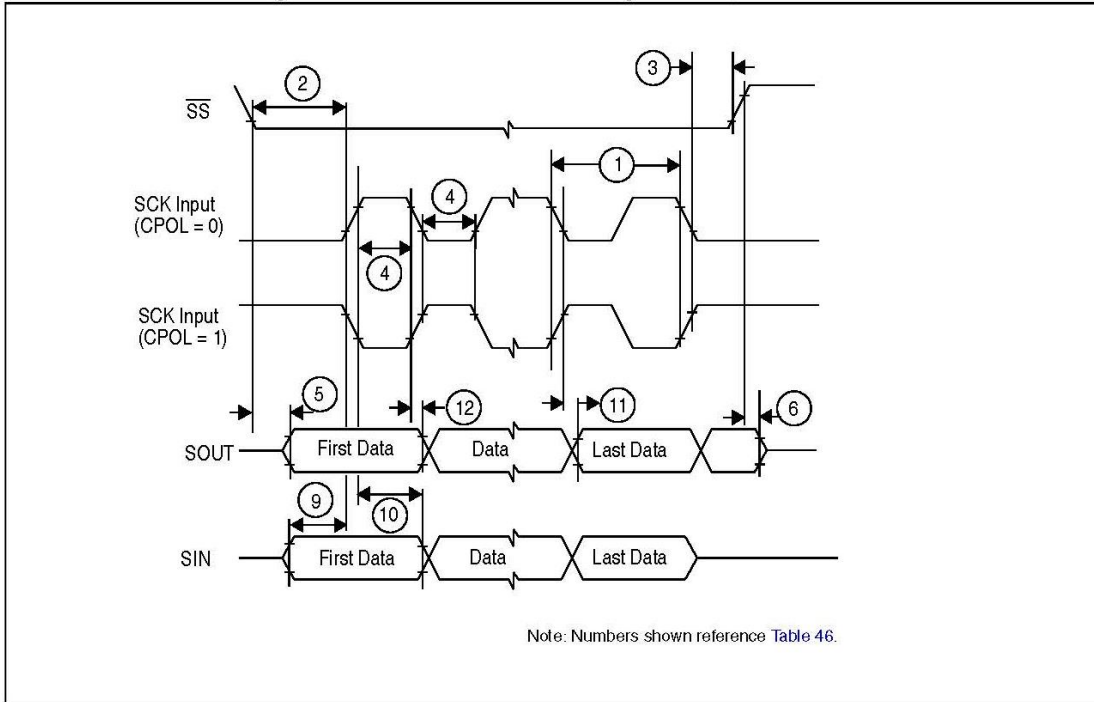


Figure 25. DSPI classic SPI timing — slave, CPHA = 1

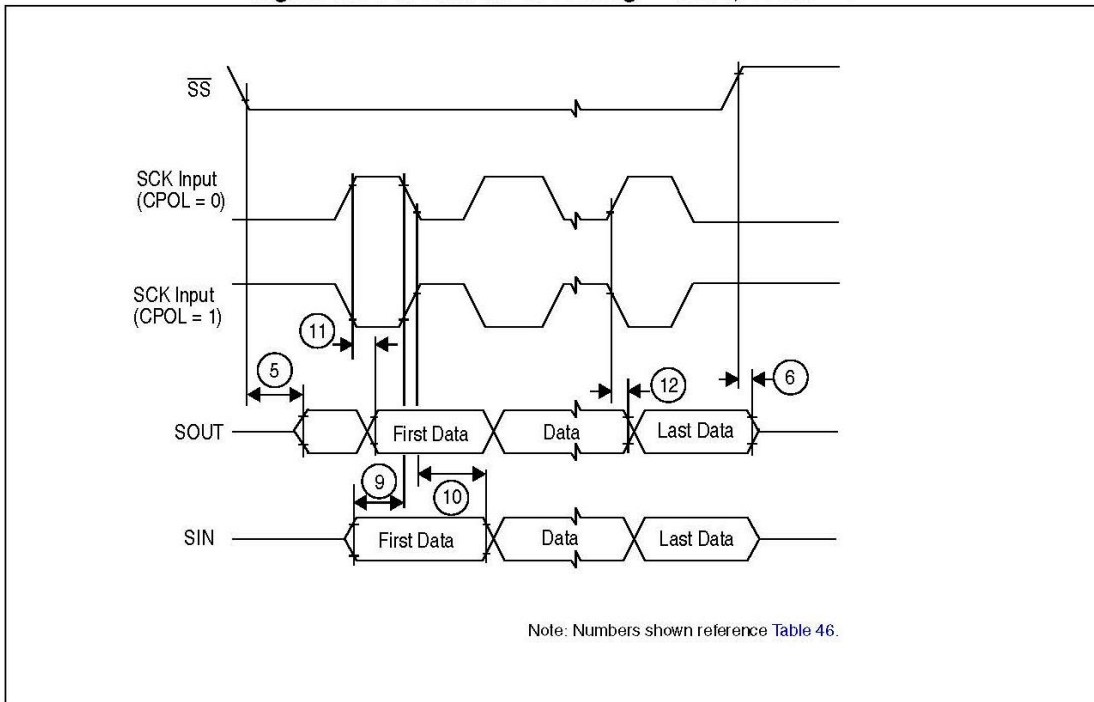


Figure 26. DSPI modified transfer format timing — master, CPHA = 0

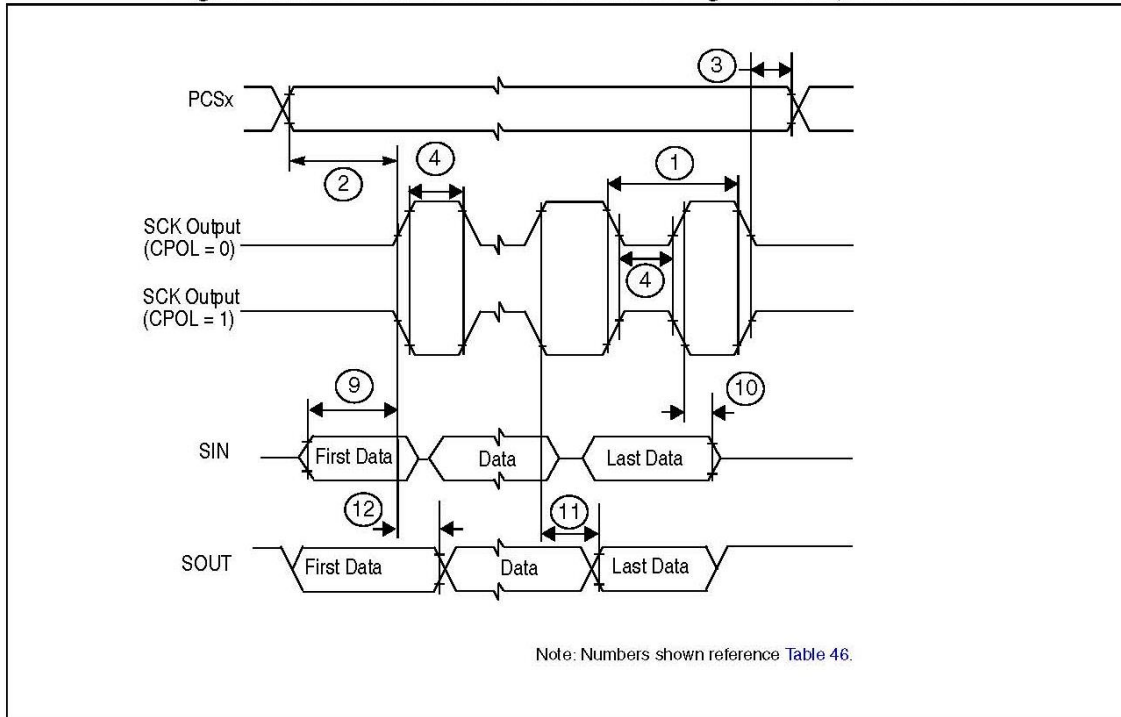


Figure 27. DSPI modified transfer format timing — master, CPHA = 1

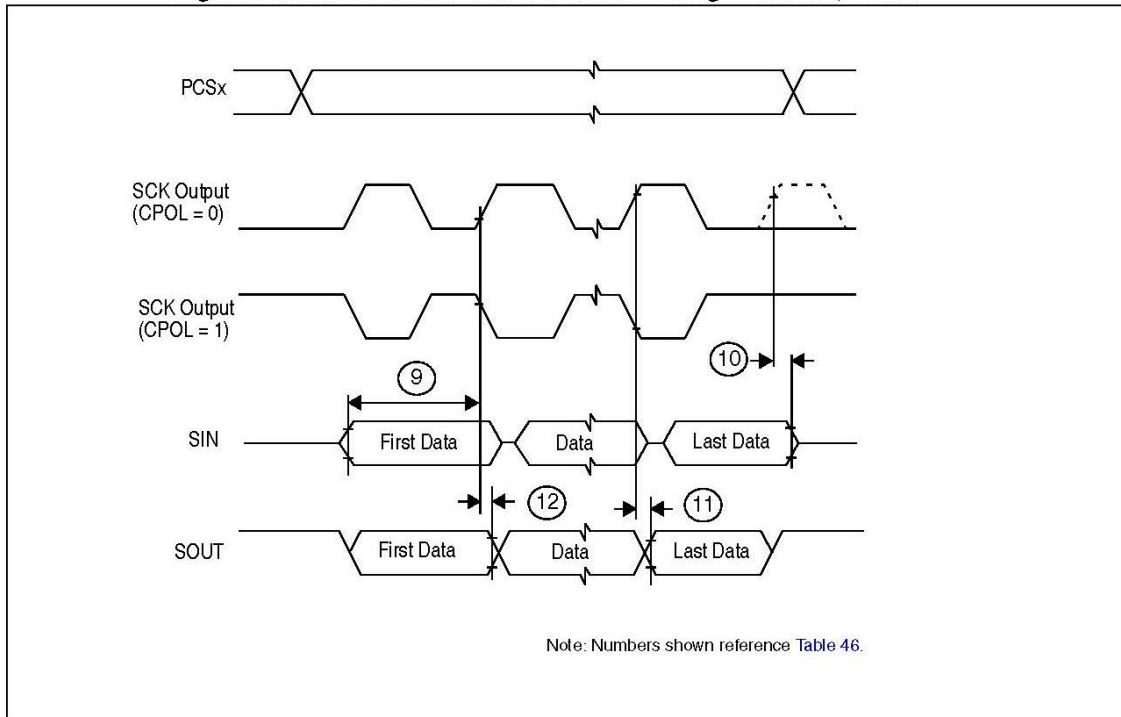


Figure 28. DSPI modified transfer format timing — slave, CPHA = 0

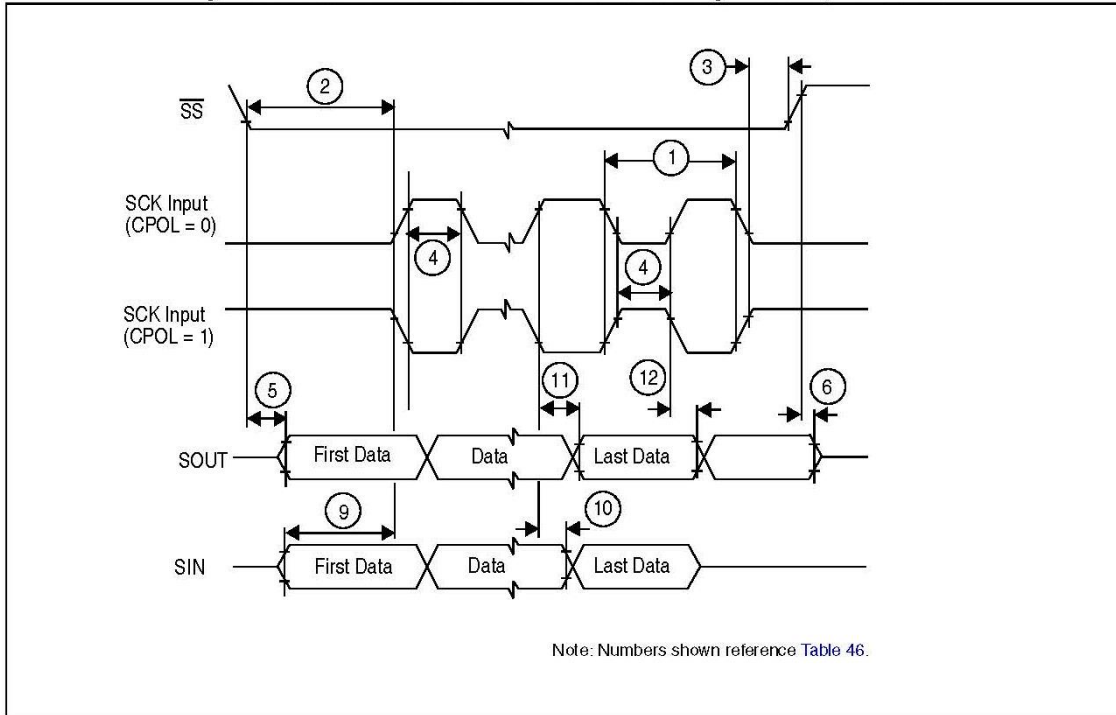
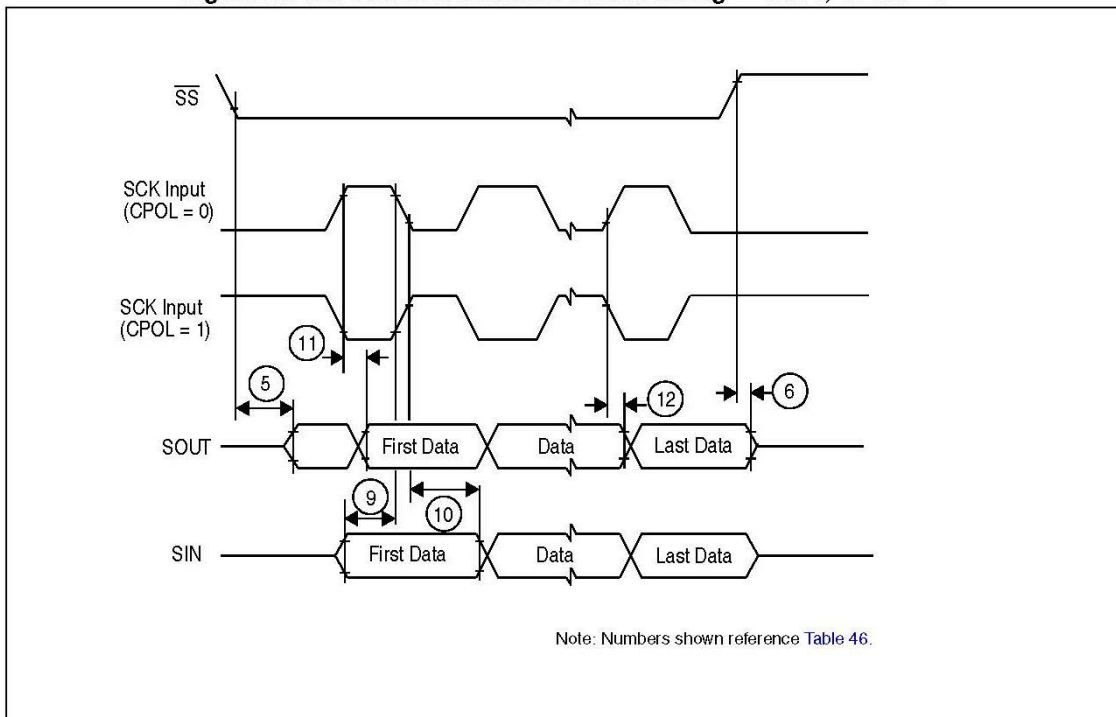
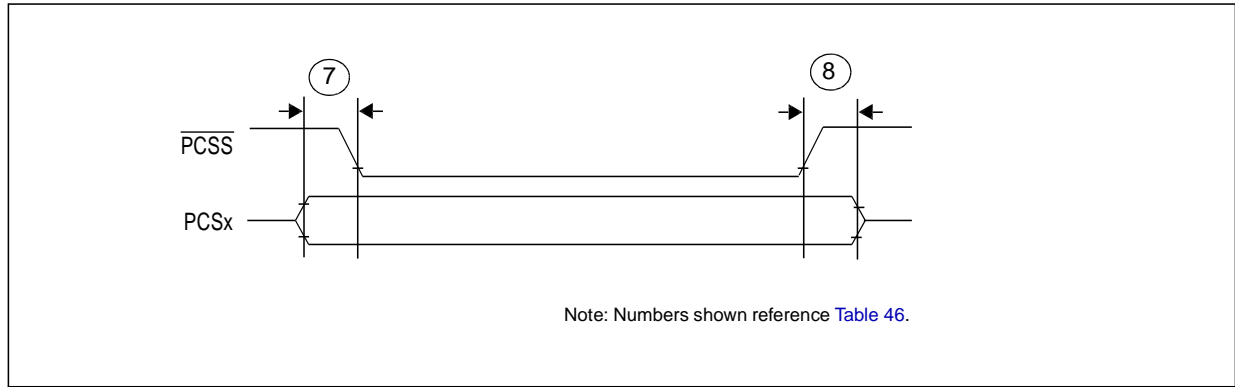


Figure 29. DSPI modified transfer format timing — slave, CPHA = 1



Figure 30. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

4.17.3 Nexus characteristics

Table 48. Nexus characteristics

No.	Symbol	C	Parameter	Value			Unit	
				Min	Typ	Max		
1	$t_{\text{TCCY}}C$	CC	D	TCK cycle time	64	—	—	ns
2	$t_{\text{MCCY}}C$	CC	D	MCKO cycle time	32	—	—	ns
3	t_{MDOV}	CC	D	MCKO low to MDO data valid	—	—	8	ns
4	t_{MSEOV}	CC	D	MCKO low to MSEO_b data valid	—	—	8	ns
5	t_{EVTOV}	CC	D	MCKO low to EVTO data valid	—	—	8	ns
6	t_{NTDIS}	CC	D	TDI data setup time	15	—	—	ns
	t_{NTMSS}	CC	D	TMS data setup time	15	—	—	ns
7	t_{NTDIH}	CC	D	TDI data hold time	5	—	—	ns
	t_{NTMSH}	CC	D	TMS data hold time	5	—	—	ns
8	t_{TDOV}	CC	D	TCK low to TDO data valid	35	—	—	ns
9	t_{TDOI}	CC	D	TCK low to TDO data invalid	6	—	—	ns

Electrical characteristics

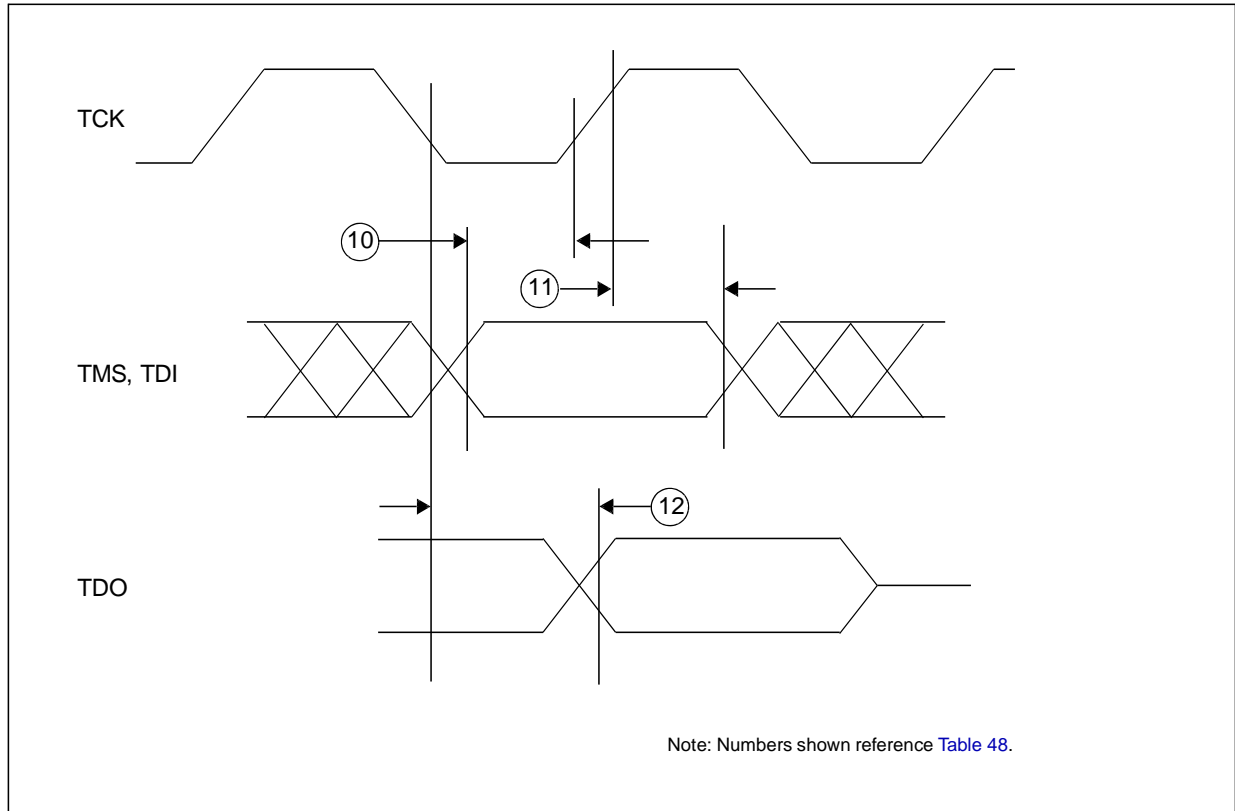


Figure 31. Nexus TDI, TMS, TDO timing

4.17.4 JTAG characteristics

Table 49. JTAG characteristics

No.	Symbol	C	Parameter	Value			Unit	
				Min	Typ	Max		
1	t_{JCYC}	CC	D	TCK cycle time	64	—	—	ns
2	t_{TDIS}	CC	D	TDI setup time	15	—	—	ns
3	t_{TDIH}	CC	D	TDI hold time	5	—	—	ns
4	t_{TMSS}	CC	D	TMS setup time	15	—	—	ns
5	t_{TMSh}	CC	D	TMS hold time	5	—	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO valid	—	—	33	ns
7	t_{TDOI}	CC	D	TCK low to TDO invalid	6	—	—	ns

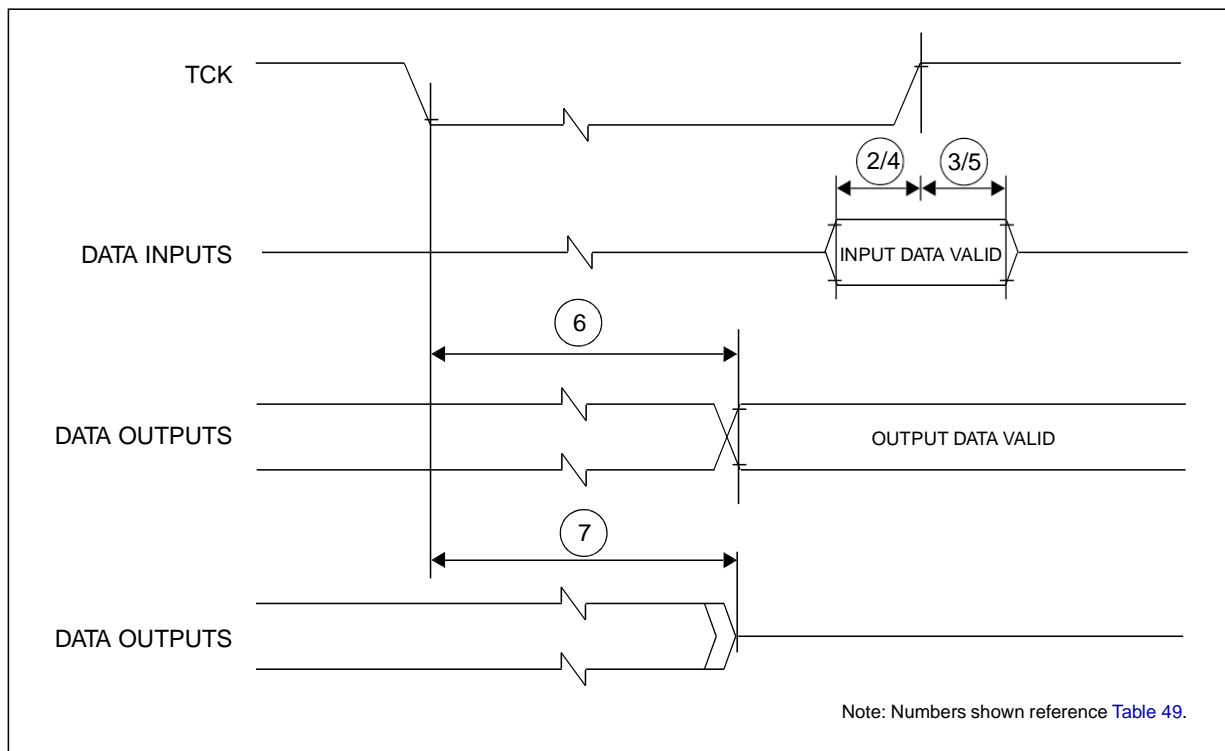
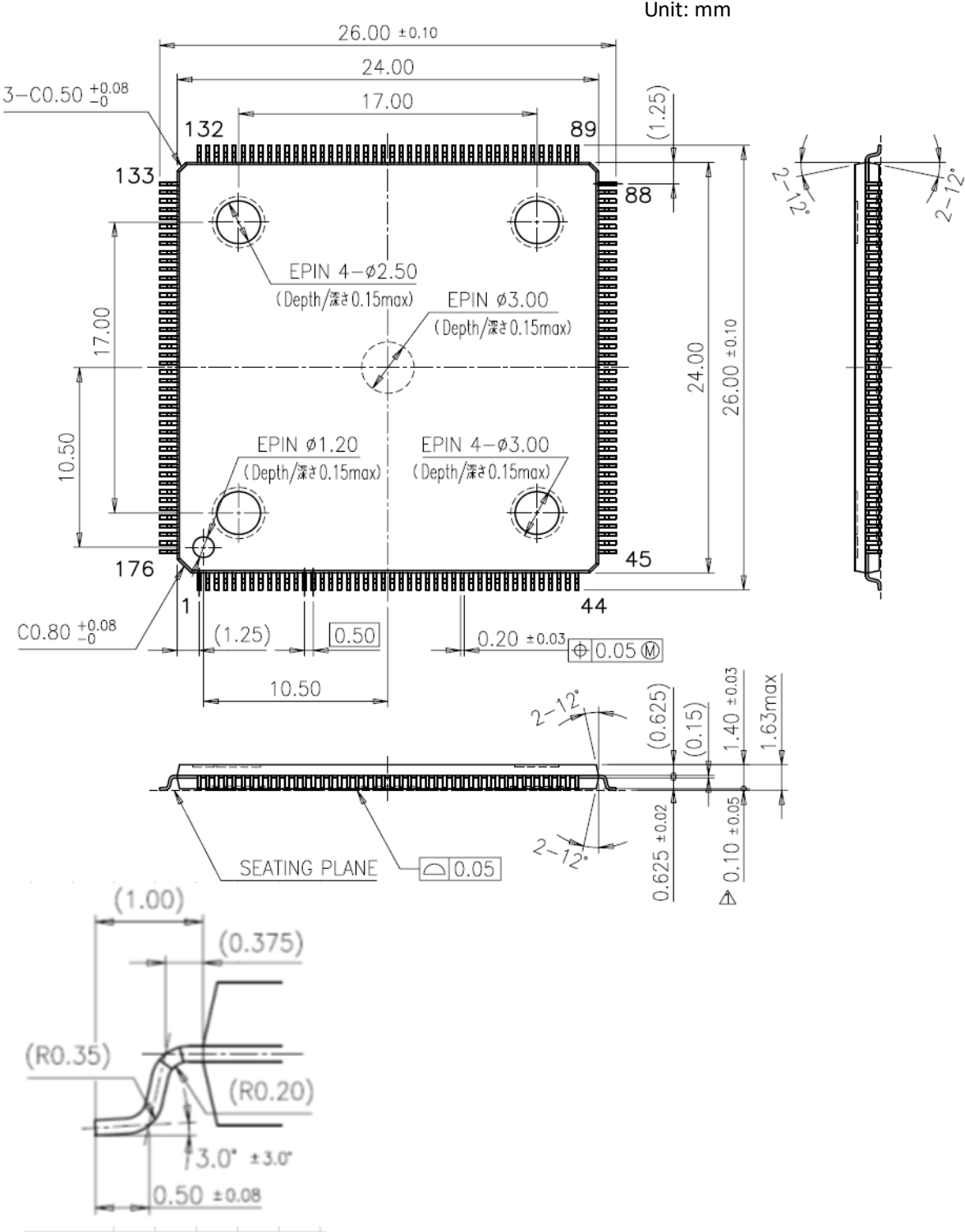


Figure 32. Timing diagram — JTAG boundary scan

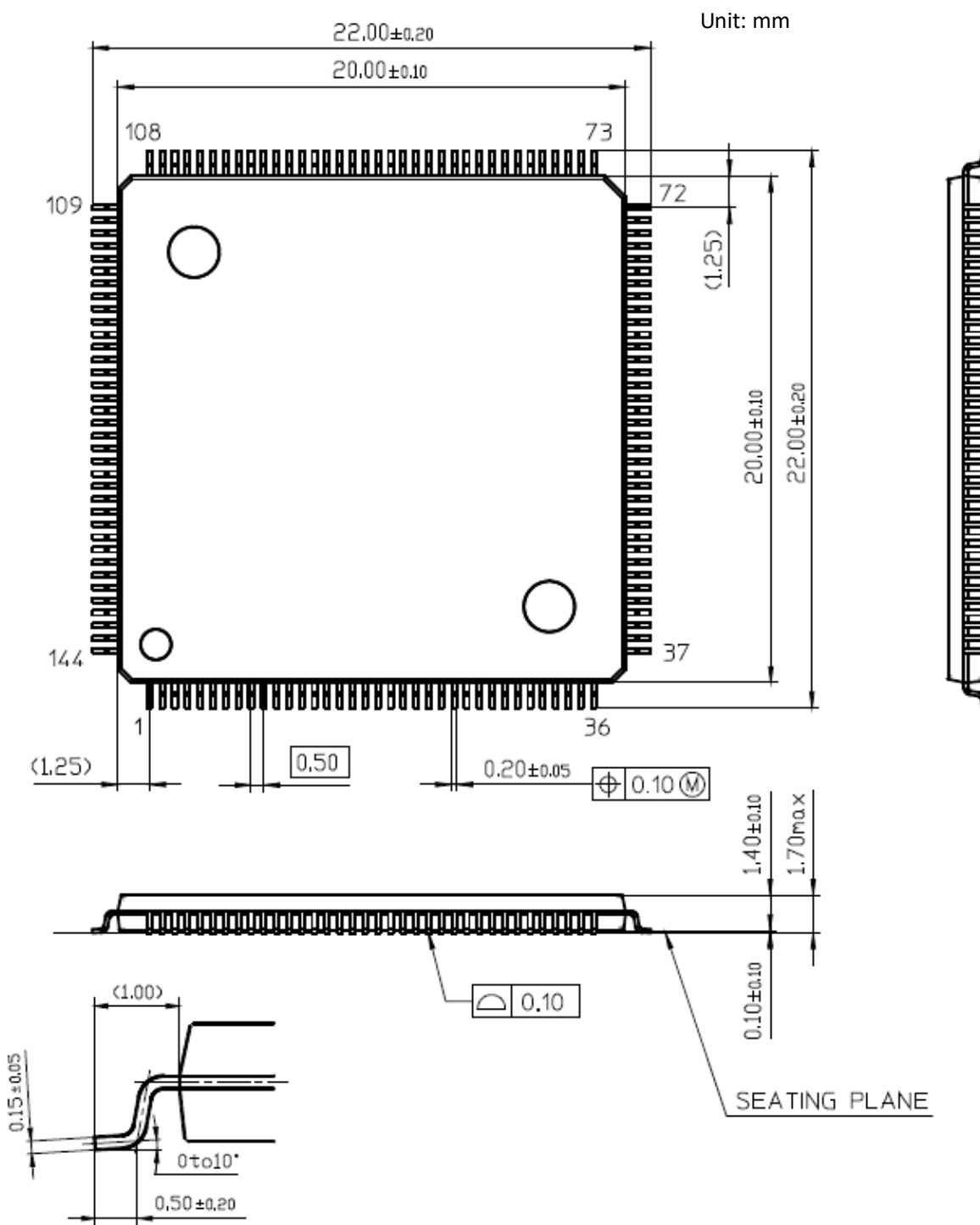
5 Package characteristics

5.1 Package mechanical data

5.1.1 176 LQFP

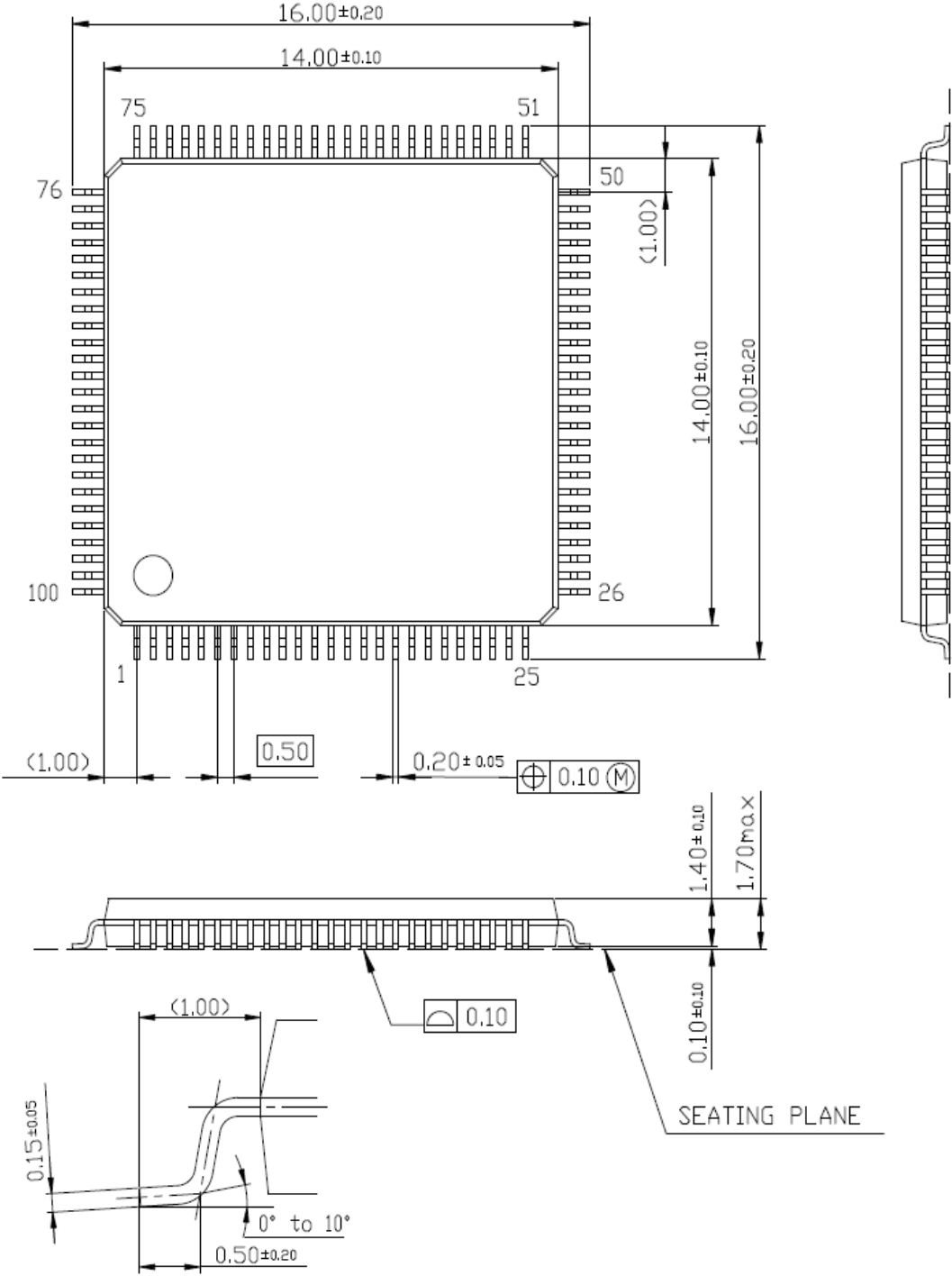


Package characteristics
5.1.2 144 LQFP



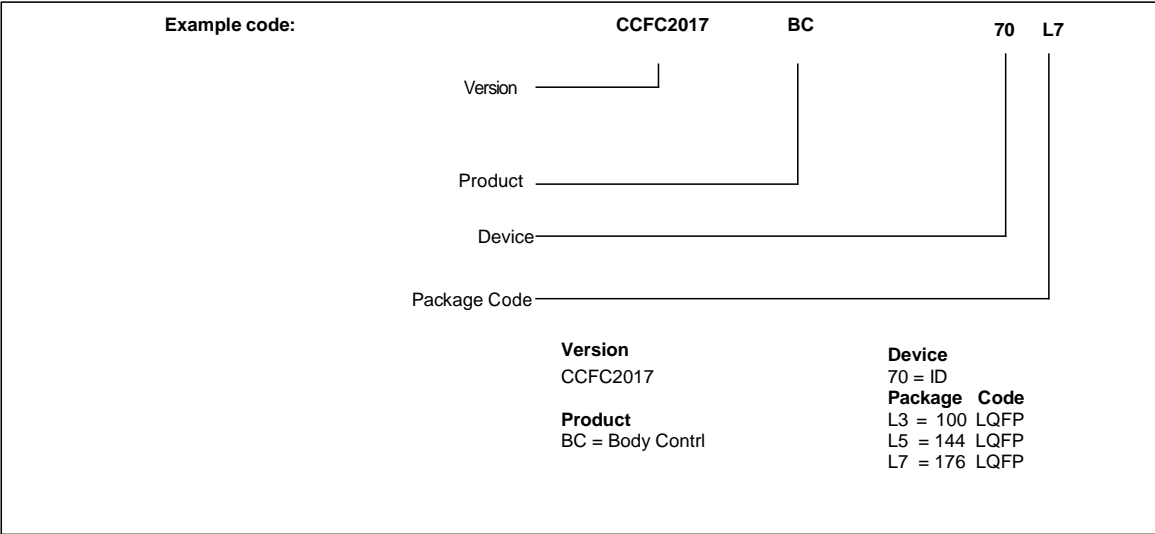
5.1.3 100 LQFP

Unit: mm



6 Ordering information

Figure 43. Commercial product code structure



7 Revision history

Table 54 summarizes revisions to this document.

Table 54. Revision history

Revision	Date	Substantive changes
1.0	2022/10/22	Initial release(Electrical characteristics shall be subject to the actual measurement)
1.1	2023/4/19	Increase Flexlin, DSPI, I2C number to MAX Modify Functional port pins I2C name to I2C_0, I2C_1, I2C_2, I2C_3 Fast external crystal oscillator change to (4 to 20 MHz) from (4 to 16 MHz)
1.2	2023/6/25	PA[8] AF1 change form E0UC[7] to E0UC[8] PD[11] EPUB change to ETPUB PH[5] add LIN11RX input
1.3	2024/05/30	Update power consumption value Update Recommended operating conditions
1.4	2024/06/07	Update power consumption value

Appendix A Abbreviations

Table 53 lists abbreviations used but not defined elsewhere in this document.

**Table 53.
Abbreviations**

Abbreviation	Meaning
CMOS	Complementary metal oxide semiconductor
CPHA	Clock phase
CPOL	Clock polarity
CS	Peripheral chip select
EVTO	Event out
MCKO	Message clock out
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
SCK	Serial communications clock
SOUT	Serial data out
TBD	To be defined
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select