CCFC2010BC Microcontroller Data Sheet(V2.2)

Features

- Single issue, 32-bit CPU core complex (c2003)
  - Compliant with the Power Architecture® technology embedded category
  - Enhanced instruction set allowing variable length encoding (VLE) for code size footprint reduction. With the optional encoding of mixed 16-bit and 32-bit instructions, it is possible to achieve significant code size footprint reduction.
- Up to 256KB on-chip code flash memory supported with the flash memory controller
- 64KB on-chip data flash memory with ECC
- Up to 32 KB on-chip SRAM
- Memory protection unit (MPU) with 8 region descriptors and 32-byte region granularity on certain family members (Refer to Table 1 for details.)
- Interrupt controller (INTC) capable of handling 231 selectable-priority interrupt sources
- Frequency modulated phase-locked loop (FMPLL)
- Crossbar switch architecture for concurrent access to peripherals, Flash, or RAM from multiple bus masters
- 16-channel eDMA controller with multiple transfer request sources using DMA multiplexer
- Boot assist module (BAM) supports internal Flash programming via a serial link (CAN or SCI)
- Timer supports I/O channels providing a range of 16-bit input capture, output compare, and pulse width modulation functions (eMIOS)
- 1 analog-to-digital converters (ADC): one 10-bit
- Cross Trigger Unit to enable synchronization of ADC conversions with a timer event from the eMIOS or PIT
- Up to 2 serial peripheral interface (DSPI) modules
- Up to 3 serial communication interface (LINFlex) modules
- Up to 2 enhanced full CAN (FlexCAN) modules with configurable buffers, each can interface compatible with canfd interface.
- 1 inter-integrated circuit (I^2C) interface module
- Up to 79 configurable general purpose pins supporting input and output operations (package dependent)
- Real-Time Counter (RTC)
- Clock source from internal 128 kHz or 16 MHz oscillator supporting autonomous wakeup with 1 ms resolution with maximum timeout of 2 seconds
- Optional support for RTC with clock source from external 32 kHz crystal oscillator, supporting wakeup with 1 sec resolution and maximum timeout of 1 hour
- Up to 8 periodic interrupt timers (PIT) with 32-bit counter resolution
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 Class Two Plus
- Device/board boundary scan testing supported per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)
- On-chip voltage regulator (VREG) for regulation of input supply for all internal levels

1 Introduction

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device.

1.1 Description

This family of 32-bit system-on-chip (SoC) microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding family of automotive-focused products designed to address the next wave of body electronics applications within the vehicle.

The advanced and cost-efficient c2003 host processor core of this automotive controller family complies with the Power Architecture technology and only implements the VLE (variable-length encoding) APU (Auxiliary Processor Unit), providing improved code density. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

Table 1. CCFC2010BC family comparison

NO.	Version / Function	CCFC2010BC30L3	CCFC2010BC30L1	CCFC2010BC30LF	CCFC2010BC30QD	CCFC2010BC20L1	CCFC2010BC20LF	CCFC2010BC20QD
1	CPU	C2003(compatible with e200z3)	C2003(compatible with e200z3)	C2003(compatible with e200z3)	C2003(compatible with e200z3)	C2003(compatible with e200z3)	C2003(compatible with e200z3)	C2003(compatible with e200z3)
2	Frequence	80Mhz	80Mhz	64Mhz	64Mhz	64Mhz	64Mhz	64Mhz
3	CFLASH	256K	256K	256K	256K	128K	128K	128K
4	DFLASH	64K	64K	64K	64K	64K	64K	64K
5	SRAM	32K	32K	32K	32K	32K	32K	32K
6	PLL	FMPLL	FMPLL	FMPLL	FMPLL	FMPLL	FMPLL	FMPLL
7	eDMA	16	16	16	16	16	16	16
8	FlexCAN	6	3	3	1	3	3	1
9	DSPI	3	2	2	2	2	2	2
10	LINFlex	6	6	4	2	6	4	2
11	eMIOS	37	19	16	10	19	16	10
12	ADC	33ch	16ch	10ch	10ch	16ch	10ch	10ch
13	PIT	8	8	8	8	8	8	8
14	STM+SWT	5	5	5	5	5	5	5
15	I2C	1	1	1	1	1	1	1
16	MPU	8	8	8	8	8	8	8
17	GPIO	79	45	29	23	45	29	23
18	Package	LQFP100	LQFP64	TQFP48	QFN32	LQFP64	TQFP48	QFN32
19	Pin	SPC5602BK0MLL	SPC5602BK0MLH	-	-	-	-	-
20	replaceability	SPC560D40L3/ S32K142*	SPC560D40L1/ S32K142*	S9S12G240*/ S32K118*/116*	S32K116*	SPC560D40L1/ S32K142*	S9S12G240*/ S32K118*/116*	S32K116*
21	reliability	AEC-Q100	AEC-Q100	AEC-Q100	AEC-Q100	AEC-Q100	AEC-Q100	AEC-Q100

2 Block diagram

Figure 1 shows a top-level block diagram of the CCFC2010BC.

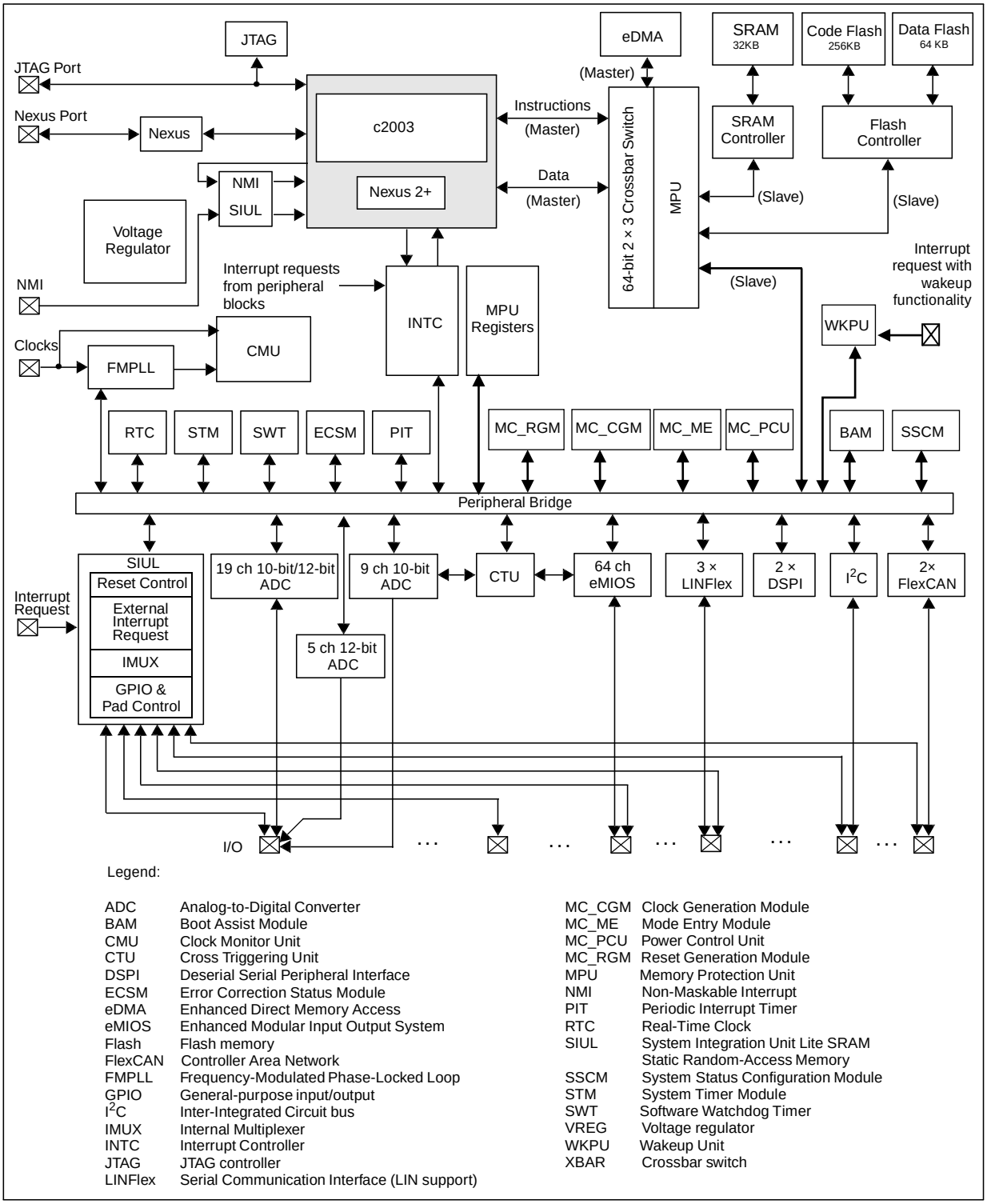


Figure 1. CCFC2010BC block diagram

Table 2 summarizes the functions of the blocks present on the CCFC2010BC.

Table 2. CCFC2010BC series block summary

Block	Function
Analog-to-digital converter (ADC)	Converts analog voltages to digital values
Boot assist module (BAM)	A block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Clock monitor unit (CMU)	Monitors clock source (internal and external) integrity
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Crossbar switch (XBAR)	Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Enhanced direct memory access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via "*n*" programmable channels
Enhanced modular input output system (eMIOS)	Provides the functionality to generate or measure events
Error correction status module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexCAN (controller area network)	Supports the standard CAN communications protocol
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Inter-integrated circuit (I^2C) bus	Two-wire bidirectional serial bus that provides a simple and efficient method of data exchange between devices
Internal multiplexer (IMUX) SIU subblock	Allows flexible mapping of peripheral interface on the different pins of the device
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller (JTAGC)	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Memory protection unit (MPU)	Provides hardware access control for all memory references generated in a device
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and modetransition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Non-maskable interrupt (NMI)	Handles external events that must produce an immediate response, such as power down detection

Table 2. CCFC2010BC series block summary (continued)

Block	Function
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called “power domains” which are controlled by the PCU
Real-time counter (RTC)	A free running counter used for time keeping applications, the RTC can be configured to generate an interrupt at a predefined interval independent of the mode of operation (run mode or low-power mode)
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System integration unit lite (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status and configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR (Automotive Open System Architecture) and operating system tasks
Software watchdog timer (SWT)	Provides protection from runaway code
Wakeup unit (WKPU)	The wakeup unit supports up to 27 external sources that can generate interrupts or wakeup events, of which 1 can cause non-maskable interrupt requests or wakeup events.

3 Signal description

3.1 Package pinouts

Figure 2, Figure 3, Figure 4, Figure 5 Figure 6 and Figure 7 show the location of the signals on the packages that this chip is available in.

For more information on pin multiplexing on this chip, see Table 3 through Table 6.

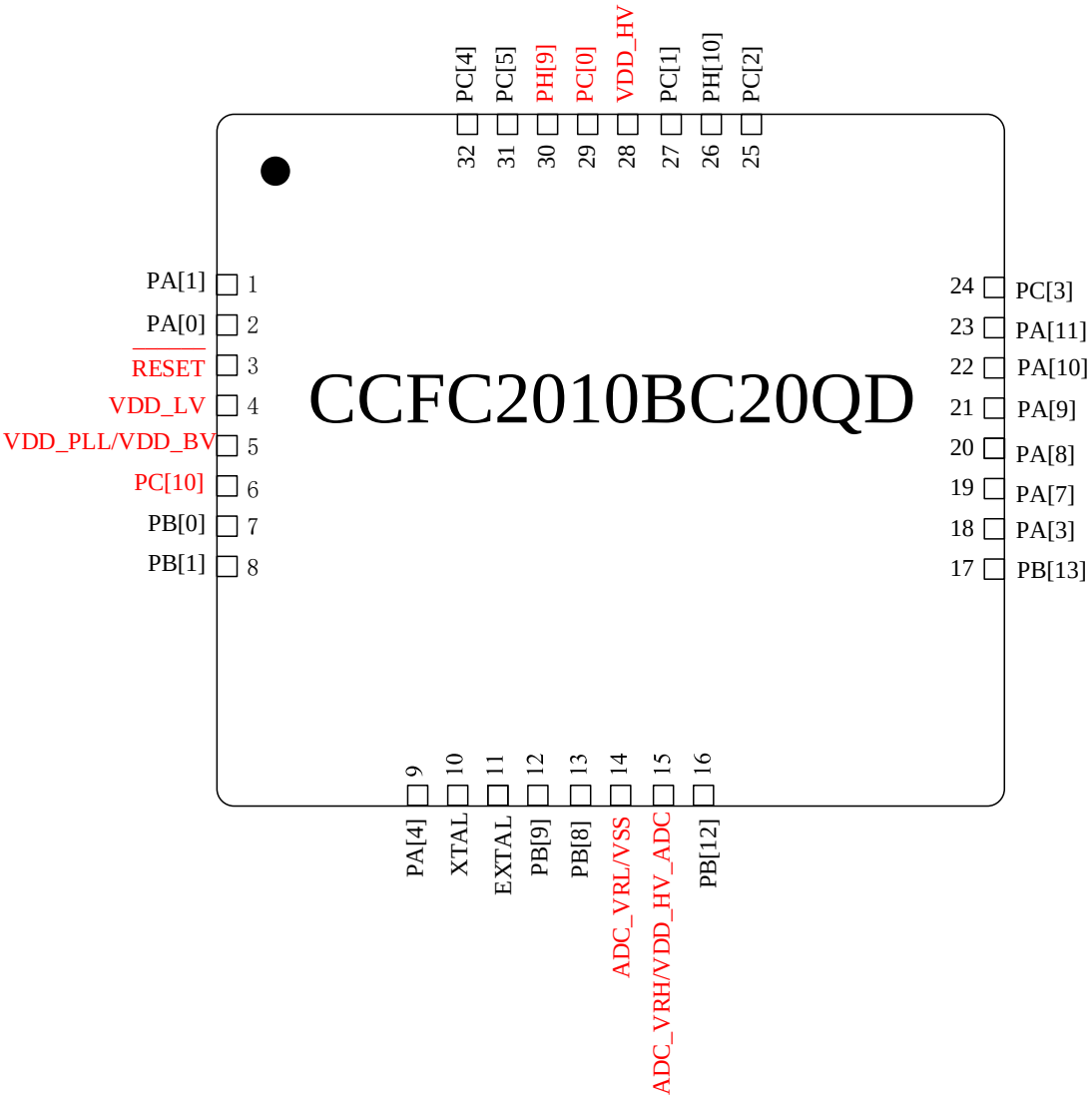


Figure 2. CCFC2010BC20QD 32-pin QFN pinout

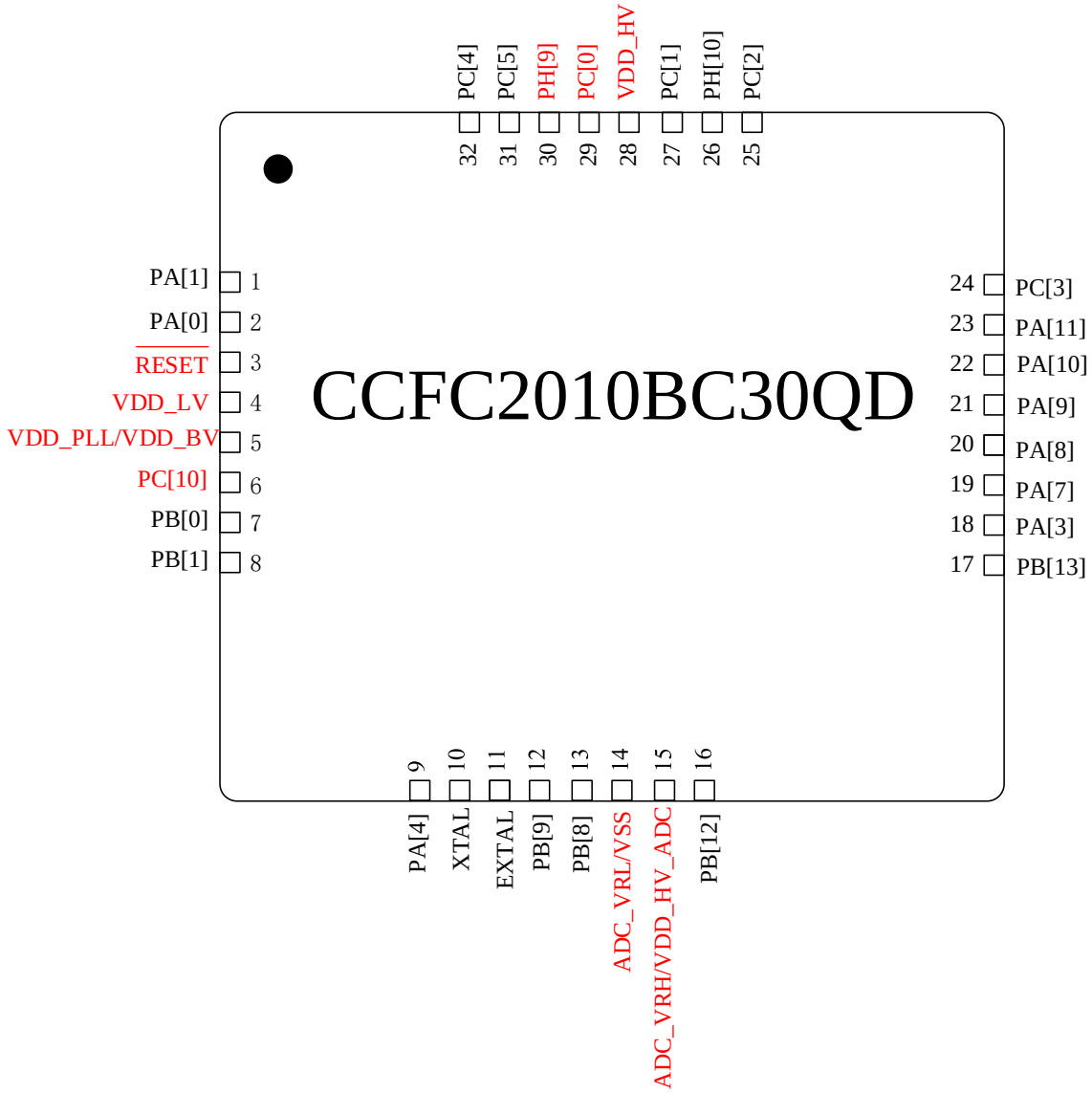


Figure 3. CCFC2010BC30QD 32-pin QFN pinout

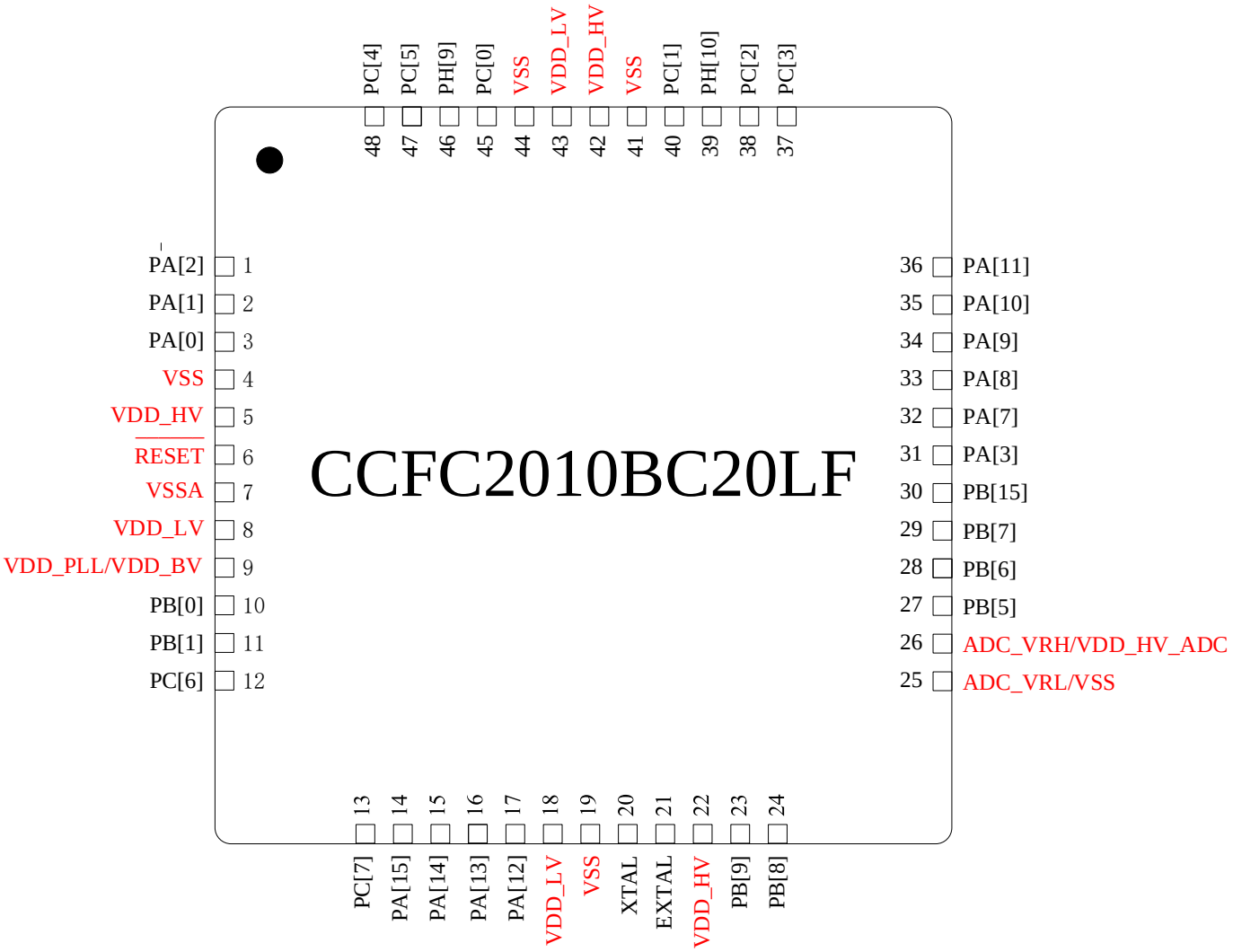


Figure 4. CCFC2010BC20LF 48-pin TQFP pinout

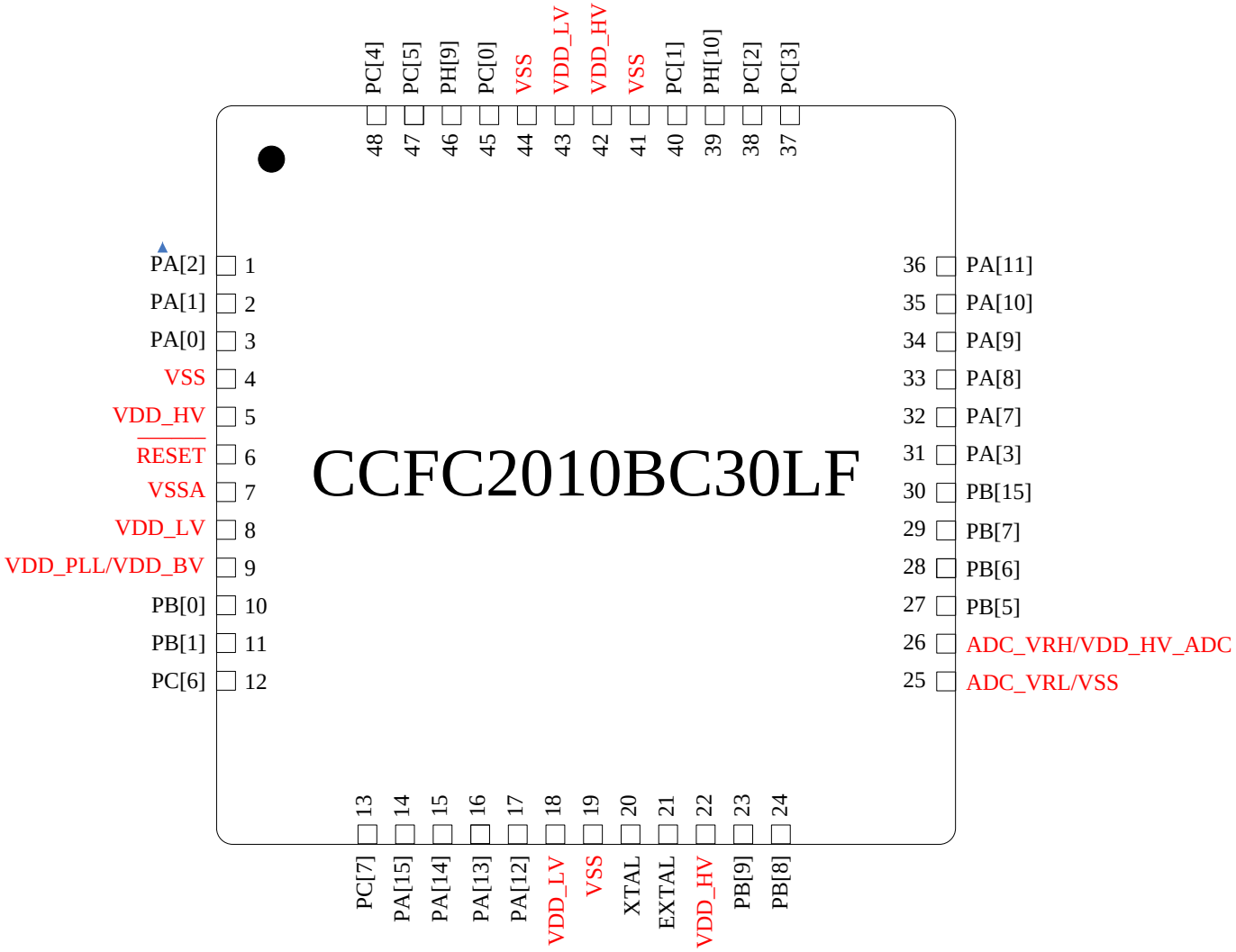


Figure 5. CCFC2010BC30LF 48-pin TQFP pinout

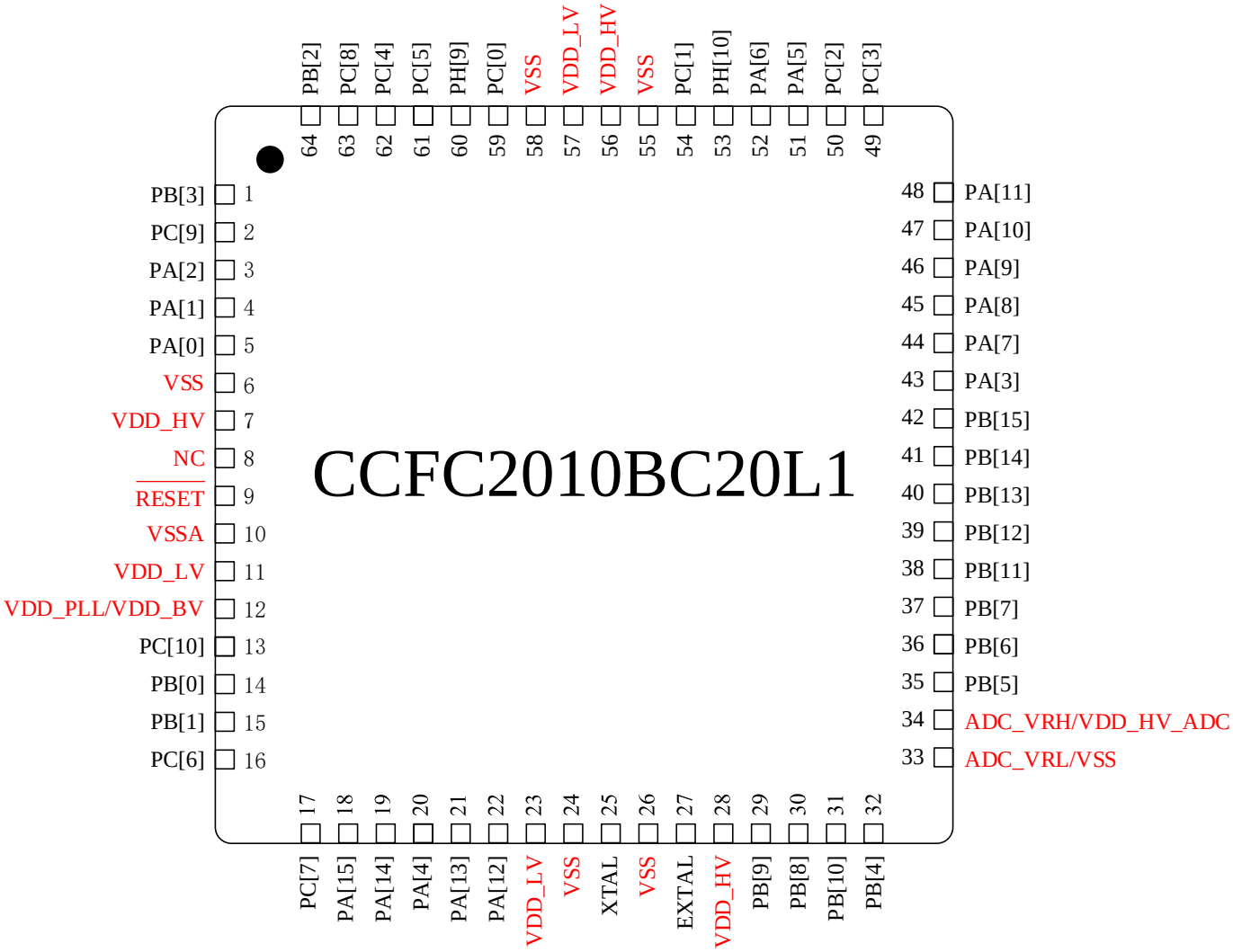


Figure 6 CCFC2010BC20L1 64-pin LQFP pinout

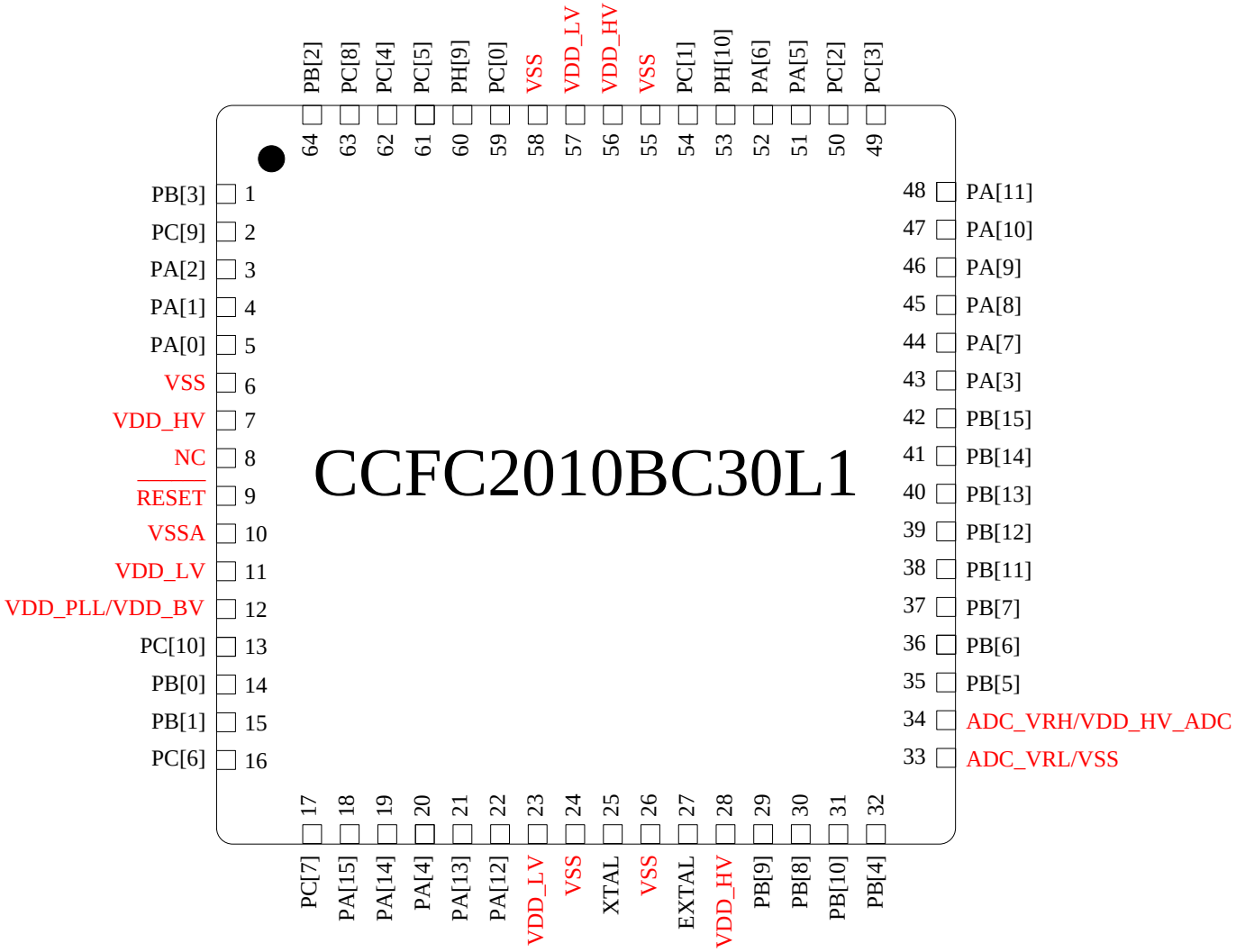


Figure 7. CCFC2010BC30L1 64-pin LQFP pinout

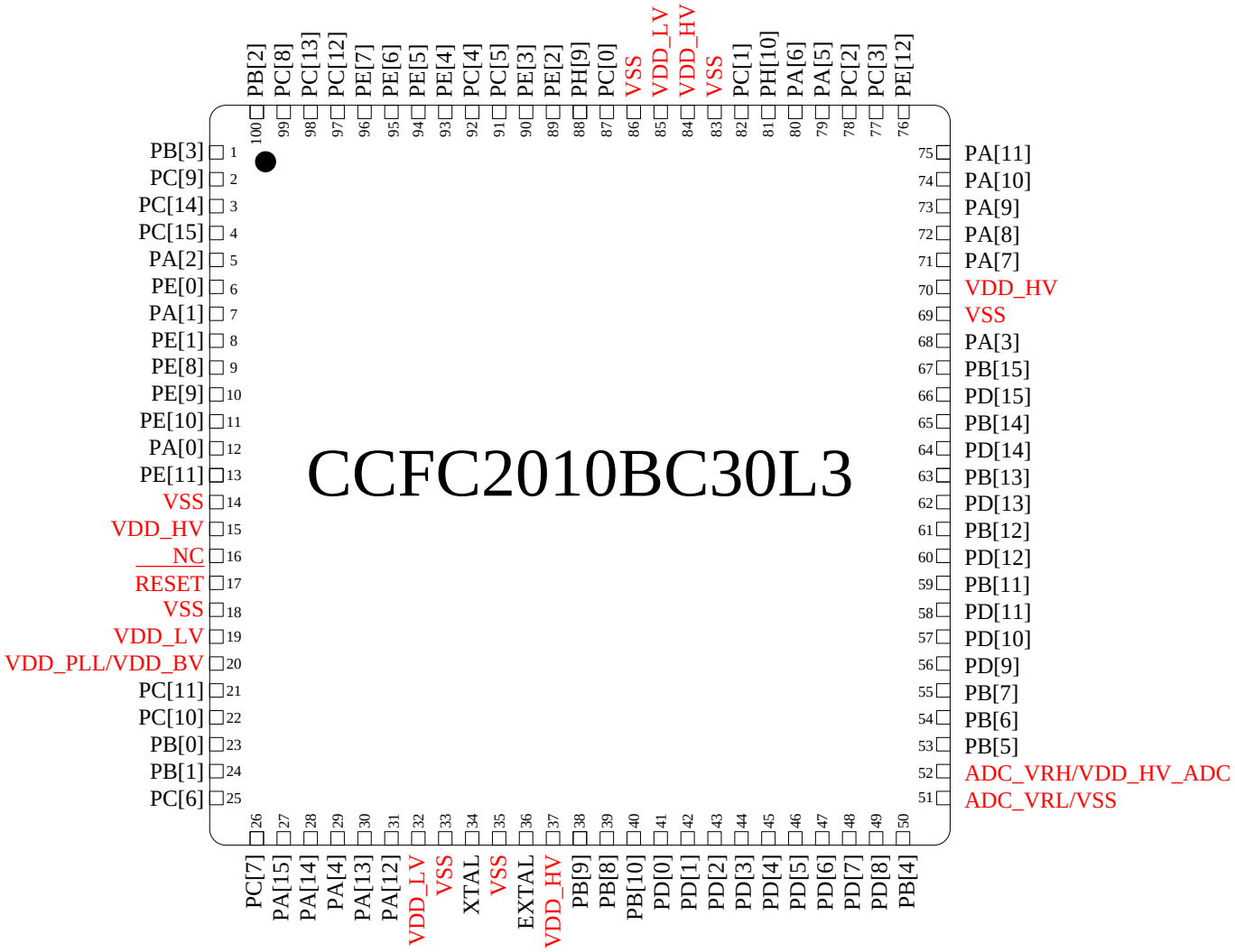


Figure 8. CCFC2010BC30L3 100-pin LQFP pinout

3.2 Pad configuration during reset phases

All pads have a fixed configuration under reset.

During the power-up phase, all pads are forced to tristate.

After power-up phase, all pads are tristate with the following exceptions:

- PA[9] (FAB) is pull-down. Without external strong pull-up the device starts fetching from flash.
- PA[8] and PC[0] are in input weak pull-up when out of reset.
- RESET pad is driven low by the device till 40 FIRC clock cycles after phase2 completion. Minimum phase3 duration is 40 FIRC cycles.
- Nexus output pads (MDO[n], MCKO, EVTO, MSEO) are forced to output.

3.3 Pad configuration during standby mode exit

Pad configuration (input buffer enable, pull enable) for low -power wakeup pads is controlled by both the SIUL and WKPU modules. During standby exit, all low power pads PA[0,1,2,4,15], PB[1,3,8,9,10]1, PC[7,9,11], PD[0,1]are configured according to their respective configuration done in the WKPU module. All other pads will have the same configuration as expected after a reset.

The TDO pad has been moved into the STANDBY domain in order to allow low-power debug handshaking in STANDBY mode. However, no pull-resistor is active on the TDO pad while in STANDBY mode. At this time the pad is configured as an input. When no debugger is connected the TDO pad is floating causing additional current consumption.

To avoid the extra consumption TDO must be connected. An external pull-up resistor in the range of 47–100 kOhms should be added between the TDO pin and VDD. Only if the TDO pin is used as an application pin and a pull-up cannot be used should a pull-down resistor with the same value be used instead between the TDO pin and GND.

3.4 Voltage supply pins

Voltage supply pins are used to provide power to the device. Three dedicated pins are used for 1.2 V regulator stabilization.

Table 3. Voltage supply pin descriptions

Port pin	Function	Pin number			
		100 LQFP	**48 TQFP**	**64 LQFP**	**32 QFN**
VDD_HV	Digital supply voltage	15, 37, 52,70, 84	22,26,42	7,28,34,56	28
VSS	Digital ground	14, 18, 33,35,51,6 9,83,86	4,7,19, 25,41,44	6,10,24,26, 33,55,58	leadframe
VDD_LV	1.2 V decoupling pins. Decoupling capacitor must be connected between these pins and the nearest V_{SS_LV} pin.[1]	19, 32, 85	8,18,43	11,23,57	4

1. PB[8, 9] ports have wakeup functionality in all modes except STANDBY.

Table 3. Voltage supply pin descriptions (continued)

Port pin	Function	Pin number			
		100 LQFP	48 TQFP	64 LQFP	32 QFN
VDD_BV	Internal regulator supply voltage	20	9	12	5
ADC_VRL	Reference ground and analog ground for the A/D converter	51	25	33	14
ADC_VRH	Reference voltage and analog supply for the A/D converter	52	26	34	15

3.5 Pad types

In the device the following types of pads are available for system pins and functional port pins:

S = Slow[1]
M = Medium[1 2]
F = Fast[1 2]
I = Input only with analog feature[1]
J = Input/Output ('S' pad) with analog feature
X = Oscillator

3.6 System pins

The system pins are listed in Table 4.

1. See the I/O pad electrical characteristics in the chip data sheet for details.
2. All medium and fast pads are in slow configuration by default at reset and can be configured as fast or medium. The only exception is PC[1] which is in medium configuration by default (see the PCR.SRC description in the chip reference manual, Pad Configuration Registers (PCR0—PCR76)).

Table 4. System pin descriptions

Port pin	Function	I/O direction	Pad type	RESET config.	Pin number			
					100 LQFP	48 TQFP	64 LQFP	32 QFN
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt-Trigger characteristics and noise filter.	I/O	M	Input weak pull-up after RGM PHASE2 and 40 FIRC cycles	17	6	9	3
EXTAL	Analog output of the oscillator amplifier circuit, when the oscillator is not in bypass mode. Analog input for the clock generator when the oscillator is in bypass mode.	I/O	X	Tristate	36	21	27	11
XTAL	Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator bypass mode is used.	I	X	Tristate	34	20	25	10

3.7 Functional port pins

The functional port pins are listed in Table 5.

Table 5. Functional port pin descriptions

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET	Pin number[4]			
								100 LQFP	48 TQFP	64 LQFP	32 QFN
Port A											
PA[0]	PCR[0]	AF0 AF1 AF2 AF3 —	GPIO[0] E0UC[0] CLKOUT E0UC[13] WKPU[19][5]	SIUL eMIOS_0 MC_CGM eMIOS_0 WKPU	I/O I/O O I/O I	M	Tristate	12	3	5	2
PA[1]	PCR[1]	AF0 AF1 AF2 AF3 —	GPIO[1] E0UC[1] NMI[6] — WKPU[2][5]	SIUL eMIOS_0 WKPU — WKPU	I/O I/O I — I	S	Tristate	7	2	4	1
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 —	GPIO[2] E0UC[2] — MA[2] WKPU[3][5]	SIUL eMIOS_0 — ADC_0 WKPU	I/O I/O — O I	S	Tristate	5	1	3	—

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.[3]	Pin number[4]			
								100 LQFP	48 TQFP	64 LQFP	32 QFN
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 — —	GPIO[3] E0UC[3] LIN5TX CS4_1 EIRQ[0] ADC1_S[0]	SIUL eMIOS_0 LINFlex_5 DSPI_1 SIUL ADC_1	I/O I/O O O I I	J	Tristate	68	31	43	18
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 — —	GPIO[4] E0UC[4] — CS0_1 LIN5RX WKPU[9][5]	SIUL eMIOS_0 — DSPI_1 LINFlex_5 WKPU	I/O I/O — I/O I I	S	Tristate	29	—	20	9
PA[5]	PCR[5]	AF0 AF1 AF2 AF3	GPIO[5] E0UC[5] LIN4TX —	SIUL eMIOS_0 LINFlex_4 —	I/O I/O O —	M	Tristate	79	—	51	—
PA[6]	PCR[6]	AF0 AF1 AF2 AF3 — —	GPIO[6] E0UC[6] — CS1_1 EIRQ[1] LIN4RX	SIUL eMIOS_0 — DSPI_1 SIUL LINFlex_4	I/O I/O — O I I	S	Tristate	80	—	52	—
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 — —	GPIO[7] E0UC[7] LIN3TX — EIRQ[2] ADC1_S[1]	SIUL eMIOS_0 LINFlex_3 — SIUL ADC_1	I/O I/O O — I I	J	Tristate	71	32	44	19
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — N/A[7] —	GPIO[8] E0UC[8] E0UC[14] — EIRQ[3] ABS[0] LIN3RX	SIUL eMIOS_0 eMIOS_0 — SIUL BAM LINFlex_3	I/O I/O I/O — I I I	S	Input, weak pull-up	72	33	45	20
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 N/A[7]	GPIO[9] E0UC[9] — CS2_1 FAB	SIUL eMIOS_0 — DSPI_1 BAM	I/O I/O — O I	S	Pull-down	73	34	46	21
PA[10]	PCR[10]	AF0 AF1 AF2 AF3 —	GPIO[10] E0UC[10] SDA LIN2TX ADC1_S[2]	SIUL eMIOS_0 I^2C_0 LINFlex_2 ADC_1	I/O I/O I/O O I	J	Tristate	74	35	47	22

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.[3]	Pin number[4]			
								100 LQFP	48 TQFP	64 LQFP	32 QFN
PA[11]	PCR[11]	AF0 AF1 AF2 AF3 — — —	GPIO[11] E0UC[11] SCL — EIRQ[16] LIN2RX ADC1_S[3]	SIUL eMIOS_0 I^2C_0 — SIUL LINFlex_2 ADC_1	I/O I/O I/O — I I I	J	Tristate	75	36	48	23
PA[12]	PCR[12]	AF0 AF1 AF2 AF3 — —	GPIO[12] — E0UC[28] CS3_1 EIRQ[17] SIN_0	SIUL — eMIOS_0 DSPI_1 SIUL DSPI_0	I/O — I/O O I I	S	Tristate	31	17	22	—
PA[13]	PCR[13]	AF0 AF1 AF2 AF3	GPIO[13] SOUT_0 E0UC[29] —	SIUL DSPI_0 eMIOS_0 —	I/O O I/O —	M	Tristate	30	16	21	—
PA[14]	PCR[14]	AF0 AF1 AF2 AF3 —	GPIO[14] SCK_0 CS0_0 E0UC[0] EIRQ[4]	SIUL DSPI_0 DSPI_0 eMIOS_0 SIUL	I/O I/O I/O I/O I	M	Tristate	28	15	19	—
PA[15]	PCR[15]	AF0 AF1 AF2 AF3 —	GPIO[15] CS0_0 SCK_0 E0UC[1] WKPU[10][5]	SIUL DSPI_0 DSPI_0 eMIOS_0 WKPU	I/O I/O I/O I/O I	M	Tristate	27	14	18	—
Port B											
PB[0]	PCR[16]	AF0 AF1 AF2 AF3	GPIO[16] CAN0TX E0UC[30] LIN0TX	SIUL FlexCAN_0 eMIOS_0 LINFlex_0	I/O O I/O O	M	Tristate	23	10	14	7
PB[1]	PCR[17]	AF0 AF1 AF2 AF3 — — —	GPIO[17] — E0UC[31] — WKPU[4][5] CAN0RX LIN0RX	SIUL — eMIOS_0 — WKPU FlexCAN_0 LINFlex_0	I/O — I/O — I I I	S	Tristate	24	11	15	8

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.[3]	Pin number[4]			
								100 LQFP	48 TQFP	64 LQFP	32 QFN
PB[2]	PCR[18]	AF0 AF1 AF2 AF3	GPIO[18] LIN0TX SDA E0UC[30]	SIUL LINFlex_0 I2C_0 eMIOS_0	I/O O I/O I/O	M	Tristate	100	—	64	—
PB[3]	PCR[19]	AF0 AF1 AF2 AF3 — —	GPIO[19] E0UC[31] SCL — WKPU[11][5] LIN0RX	SIUL eMIOS_0 I2C_0 — WKPU LINFlex_0	I/O I/O I/O — I I	S	Tristate	1	—	1	—
PB[4]	PCR[20]	AF0 AF1 AF2 AF3 — — —	— — — — ADC0_P[0] ADC1_P[0] GPIO[20]	— — — — ADC_0 ADC_1 SIUL	— — — — I I I	I	Tristate	50	—	32	—
PB[5]	PCR[21]	AF0 AF1 AF2 AF3 — — —	— — — — ADC0_P[1] ADC1_P[1] GPIO[21]	— — — — ADC_0 ADC_1 SIUL	— — — — I I I	I	Tristate	53	27	35	—
PB[6]	PCR[22]	AF0 AF1 AF2 AF3 — — —	— — — — ADC0_P[2] ADC1_P[2] GPIO[22]	— — — — ADC_0 ADC_1 SIUL	— — — — I I I	I	Tristate	54	28	36	—
PB[7]	PCR[23]	AF0 AF1 AF2 AF3 — — —	— — — — ADC0_P[3] ADC1_P[3] GPIO[23]	— — — — ADC_0 ADC_1 SIUL	— — — — I I I	I	Tristate	55	29	37	—

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.[3]	Pin number[4]			
								100 LQFP	48 TQFP	64 LQFP	32 QFN
PB[8]	PCR[24]	AF0 AF1 AF2 AF3 — — — —	GPIO[24] — — — OSC32K_XTAL[8] WKPU[25][5] ADC0_S[0] ADC1_S[4]	SIUL — — — OSC32K WKPU ADC_0 ADC_1	I — — — — I[9] I I	I	—	39	24	30	13
PB[9]	PCR[25]	AF0 AF1 AF2 AF3 — — — —	GPIO[25] — — — OSC32K_EXTAL[8] WKPU[26][5] ADC0_S[1] ADC1_S[5]	SIUL — — — OSC32K WKPU ADC_0 ADC_1	I — — — — I[9] I I	I	—	38	23	29	12
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 — — —	GPIO[26] — — — WKPU[8][5] ADC0_S[2] ADC1_S[6]	SIUL — — — WKPU ADC_0 ADC_1	I/O — — — I I I	J	Tristate	40	—	31	—
PB[11]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ADC0_S[3]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — I/O I	J	Tristate	59	—	38	—
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ADC0_X[0]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	J	Tristate	61	—	39	16
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ADC0_X[1]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	J	Tristate	63	—	40	17
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ADC0_X[2]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	J	Tristate	65	—	41	—

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.[3]	Pin number[4]			
								100 LQFP	48 TQFP	64 LQFP	32 QFN
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 ADC0_X[3]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	J	Tristate	67	30	42	—
Port C											
PC[0][10]	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M	Input, weak pull-up	87	45	59	29
PC[1][10]	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO —	SIUL — JTAGC —	I/O — O —	F[11]	Tristate	82	40	54	27
PC[2]	PCR[34]	AF0 AF1 AF2 AF3	GPIO[34] SCK_1 CAN4TX DEBUG[0] EIRQ[5]	SIUL DSPI_1 FlexCAN_4 SSCM SIUL	I/O I/O O O	M	Tristate	78	38	50	25
PC[3]	PCR[35]	AF0 AF1 AF2 AF3 — —	GPIO[35] CS0_1 MA[0] DEBUG[1] EIRQ[6] CAN4RX	SIUL DSPI_1 ADC_0 SSCM SIUL FlexCAN_4	I/O I/O O O I I	S	Tristate	77	37	49	24
PC[4]	PCR[36]	AF0 AF1 AF2 AF3 — — —	GPIO[36] E1UC[31] — DEBUG[2] EIRQ[18] SIN_1 CAN3RX	SIUL eMIOS_1 — SSCM SIUL DSPI_1 FlexCAN_3	I/O I/O — O I I I	M	Tristate	92	48	62	32
PC[5]	PCR[37]	AF0 AF1 AF2 AF3 —	GPIO[37] SOUT_1 CAN3TX DEBUG[3] EIRQ[7]	SIUL DSPI_1 FlexCAN_3 SSCM SIUL	I/O O O O I	M	Tristate	91	47	61	31

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.[3]	Pin number[4]			
								100 LQFP	48 TQFP	64 LQFP	32 QFN
PC[6]	PCR[38]	AF0 AF1 AF2 AF3	GPIO[38] LIN1TX E1UC[28] DEBUG[4]	SIUL LINFlex_1 eMIOS_1 SSCM	I/O O I/O O	S	Tristate	25	12	16	—
PC[7]	PCR[39]	AF0 AF1 AF2 AF3 — —	GPIO[39] — E1UC[29] DEBUG[5] LIN1RX WKPU[12][5]	SIUL — eMIOS_1 SSCM LINFlex_1 WKPU	I/O — I/O O I I	S	Tristate	26	13	17	—
PC[8]	PCR[40]	AF0 AF1 AF2 AF3	GPIO[40] LIN2TX E0UC[3] DEBUG[6]	SIUL LINFlex_2 eMIOS_0 SSCM	I/O O I/O O	S	Tristate	99	—	63	—
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — E0UC[7] DEBUG[7] WKPU[13][5] LIN2RX	SIUL — eMIOS_0 SSCM WKPU LINFlex_2	I/O — I/O O I I	S	Tristate	2	—	2	—
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] CAN1TX CAN4TX MA[1]	SIUL FlexCAN_1 FlexCAN_4 ADC_0	I/O O O O	M	Tristate	22	—	13	6
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 — — —	GPIO[43] — — MA[2] WKPU[5][5] CAN1RX CAN4RX	SIUL — — ADC_0 WKPU FlexCAN_1 Flex CA	I/O — — O I I I	S	Tristate	21	—	—	—
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 — —	GPIO[44] E0UC[12] — — EIRQ[19] SIN_2	SIUL eMIOS_0 — — SIUL DSPI_2	I/O I/O — — I I	M	Tristate	97	—	—	—
PC[13]	PCR[45]	AF0 AF1 AF2 AF3	GPIO[45] E0UC[13] SOUT_2 —	SIUL eMIOS_0 DSPI_2 —	I/O I/O O —	S	Tristate	98	—	—	—

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.[3]	Pin number[4]			
								100 LQFP	48 TQFP	64 LQFP	32 QFN
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 —	GPIO[46] E0UC[14] SCK_2 — EIRQ[8]	SIUL eMIOS_0 DSPI_2 — SIUL	I/O I/O I/O — I	S	Tristate	3	—	—	—
PC[15]	PCR[47]	AF0 AF1 AF2 AF3 —	GPIO[47] E0UC[15] CS0_2 — EIRQ[20]	SIUL eMIOS_0 DSPI_2 — SIUL	I/O I/O I/O — I	M	Tristate	4	—	—	—
Port D											
PD[0]	PCR[48]	AF0 AF1 AF2 AF3 — — —	GPIO[48] — — — WKPU[27][5] ADC0_P[4] ADC1_P[4]	SIUL — — — WKPU ADC_0 ADC_1	I — — — I I I	I	Tristate	41	—	—	—
PD[1]	PCR[49]	AF0 AF1 AF2 AF3 — — —	GPIO[49] — — — WKPU[28][5] ADC0_P[5] ADC1_P[5]	SIUL — — — WKPU ADC_0 ADC_1	I — — — I I I	I	Tristate	42	—	—	—
PD[2]	PCR[50]	AF0 AF1 AF2 AF3 — —	GPIO[50] — — — ADC0_P[6] ADC1_P[6]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	43	—	—	—
PD[3]	PCR[51]	AF0 AF1 AF2 AF3 — —	GPIO[51] — — — ADC0_P[7] ADC1_P[7]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	44	—	—	—
PD[4]	PCR[52]	AF0 AF1 AF2 AF3 — —	GPIO[52] — — — ADC0_P[8] ADC1_P[8]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	45	—	—	—

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.[3]	Pin number[4]			
								100 LQFP	48 TQFP	64 LQFP	32 QFN
PD[5]	PCR[53]	AF0 AF1 AF2 AF3 — —	GPIO[53] — — — ADC0_P[9] ADC1_P[9]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	46	—	—	—
PD[6]	PCR[54]	AF0 AF1 AF2 AF3 — —	GPIO[54] — — — ADC0_P[10] ADC1_P[10]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	47	—	—	—
PD[7]	PCR[55]	AF0 AF1 AF2 AF3 — —	GPIO[55] — — — ADC0_P[11] ADC1_P[11]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	48	—	—	—
PD[8]	PCR[56]	AF0 AF1 AF2 AF3 — —	GPIO[56] — — — ADC0_P[12] ADC1_P[12]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	49	—	—	—
PD[9]	PCR[57]	AF0 AF1 AF2 AF3 — —	GPIO[57] — — — ADC0_P[13] ADC1_P[13]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	56	—	—	—
PD[10]	PCR[58]	AF0 AF1 AF2 AF3 — —	GPIO[58] — — — ADC0_P[14] ADC1_P[14]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	57	—	—	—
PD[11]	PCR[59]	AF0 AF1 AF2 AF3 — —	GPIO[59] — — — ADC0_P[15] ADC1_P[15]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	58	—	—	—

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.[3]	Pin number[4]			
								100 LQFP	48 TQFP	64 LQFP	32 QFN
PD[12]	PCR[60]	AF0 AF1 AF2 AF3 —	GPIO[60] CS5_0 E0UC[24] — ADC0_S[4]	SIUL DSPI_0 eMIOS_0 — ADC_0	I/O O I/O — I	J	Tristate	60	—	—	—
PD[13]	PCR[61]	AF0 AF1 AF2 AF3 —	GPIO[61] CS0_1 E0UC[25] — ADC0_S[5]	SIUL DSPI_1 eMIOS_0 — ADC_0	I/O I/O I/O — I	J	Tristate	62	—	—	—
PD[14]	PCR[62]	AF0 AF1 AF2 AF3 —	GPIO[62] CS1_1 E0UC[26] — ADC0_S[6]	SIUL DSPI_1 eMIOS_0 — ADC_0	I/O O I/O — I	J	Tristate	64	—	—	—
PD[15]	PCR[63]	AF0 AF1 AF2 AF3 —	GPIO[63] CS2_1 E0UC[27] — ADC0_S[7]	SIUL DSPI_1 eMIOS_0 — ADC_0	I/O O I/O — I	J	Tristate	66	—	—	—
Port E											
PE[0]	PCR[64]	AF0 AF1 AF2 AF3 — —	GPIO[64] E0UC[16] — — WKPU[6][5] CAN5RX	SIUL eMIOS_0 — — WKPU FlexCAN_5	I/O I/O — — I I	S	Tristate	6	—	—	—
PE[1]	PCR[65]	AF0 AF1 AF2 AF3	GPIO[65] E0UC[17] CAN5TX —	SIUL eMIOS_0 FlexCAN_5 —	I/O I/O O —	M	Tristate	8	—	—	—
PE[2]	PCR[66]	AF0 AF1 AF2 AF3 — —	GPIO[66] E0UC[18] — — EIRQ[21] SIN_1	SIUL eMIOS_0 — — SIUL DSPI_1	I/O I/O — — I I	M	Tristate	89	—	—	—
PE[3]	PCR[67]	AF0 AF1 AF2 AF3	GPIO[67] E0UC[19] SOUT_1 —	SIUL eMIOS_0 DSPI_1 —	I/O I/O O —	M	Tristate	90	—	—	—

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.[3]	Pin number[4]			
								100 LQFP	48 TQFP	64 LQFP	32 QFN
PE[4]	PCR[68]	AF0 AF1 AF2 AF3 —	GPIO[68] E0UC[20] SCK_1 — EIRQ[9]	SIUL eMIOS_0 DSPI_1 — SIUL	I/O I/O I/O — I	M	Tristate	93	—	—	—
PE[5]	PCR[69]	AF0 AF1 AF2 AF3	GPIO[69] E0UC[21] CS0_1 MA[2]	SIUL eMIOS_0 DSPI_1 ADC_0	I/O I/O I/O O	M	Tristate	94	—	—	—
PE[6]	PCR[70]	AF0 AF1 AF2 AF3 —	GPIO[70] E0UC[22] CS3_0 MA[1] EIRQ[22]	SIUL eMIOS_0 DSPI_0 ADC_0 SIUL	I/O I/O O O I	M	Tristate	95	—	—	—
PE[7]	PCR[71]	AF0 AF1 AF2 AF3 —	GPIO[71] E0UC[23] CS2_0 MA[0] EIRQ[23]	SIUL eMIOS_0 DSPI_0 ADC_0 SIUL	I/O I/O O O I	M	Tristate	96	—	—	—
PE[8]	PCR[72]	AF0 AF1 AF2 AF3	GPIO[72] CAN2TX E0UC[22] CAN3TX	SIUL FlexCAN_2 eMIOS_0 FlexCAN_3	I/O O I/O O	M	Tristate	9	—	—	—
PE[9]	PCR[73]	AF0 AF1 AF2 AF3	GPIO[73] — E0UC[23] — WKPU[7][5] CAN2RX CAN3RX	SIUL — eMIOS_0 — WKPU FlexCAN_2 FlexCAN_3	I/O — I/O — I I I	S	Tristate	10	—	—	—
PE[10]	PCR[74]	AF0 AF1 AF2 AF3 —	GPIO[74] LIN3TX CS3_1 E1UC[30] EIRQ[10]	SIUL LINFlex_3 DSPI_1 eMIOS_1 SIUL	I/O O O I/O I	S	Tristate	11	—	—	—
PE[11]	PCR[75]	AF0 AF1 AF2 AF3 — —	GPIO[75] E0UC[24] CS4_1 — LIN3RX WKPU[14][5]	SIUL eMIOS_0 DSPI_1 — LINFlex_3 WKPU	I/O I/O O — I I	S	Tristate	13	—	—	—

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.[3]	Pin number[4]			
								100 LQFP	48 TQFP	64 LQFP	32 QFN
PE[12]	PCR[76]	AF0 AF1 AF2 AF3 — — —	GPIO[76] — E1UC[19][12] — EIRQ[11] SIN_2 ADC1_S[7]	SIUL — eMIOS_1 — SIUL DSPI_2 ADC_1	I/O — I/O — I I I	J	Tristate	76	—	—	—
other											
PH[9]			— TCK —	SIUL — JTAGC —	I/O — I —	S	Input, weak pull-up	88	46	60	30
PH[10]			— TMS —	SIUL — JTAGC —	I/O — I —	M	Input, weak pull-up	81	39	53	26

[1] Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIUL module. PCR.PA = 00–> AF0; PCR.PA = 01 -> AF1; PCR.PA = 10 -> AF2; PCR.PA = 11-> AF3. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".

[2] Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.

[3] The RESET configuration applies during and after reset.

[4] 30L3 refers to CCFC2010BC30L3, 30L1 refers to CCFC2010BC30L1, 30LF refers to CCFC2010BC30LF

[5] All WKPU pins also support external interrupt capability. See the WKPU chapter for further details.

[6] NMI has higher priority than alternate function. When NMI is selected, the PCR.AF field is ignored.

[7] "Not applicable" because these functions are available only while the device is booting. Refer to the BAM information for details.

[8] Value of PCR.IBE bit must be 0

[9] This wakeup input cannot be used to exit STANDBY mode.

[10] Out of reset all the functional pins except PC[0:1] and PH[9:10] are available to the user as GPIO.
PC[0:1] are available as JTAG pins (TDI and TDO respectively).
PH[9:10] are available as JTAG pins (TCK and TMS respectively).
It is up to the user to configure these pins as GPIO when needed.

[11] PC[1] is a fast/medium pad but is in medium configuration by default. This pad is in Alternate Function 2 mode after reset which has TDO functionality. The reset value of PCR.OBE is '1', but this setting has no impact as long as this pad stays in AF2 mode. After configuring this pad as GPIO (PCR.PA = 0), output buffer is enabled as reset value of PCR.OBE = 1.

[12] Not available in 48 & 64 LQFP package

3.8 Nexus 2+ pins

Table 6. Nexus 2+ pin descriptions

Port pin	Function	I/O direction	Pad type	Function after reset
MCKO	Message clock out	O	F	—
MDO0	Message data out 0	O	M	—
MDO1	Message data out 1	O	M	—
MDO2	Message data out 2	O	M	—
MDO3	Message data out 3	O	M	—
EVTI	Event in	I	M	Pull-up
EVTO	Event out	O	M	—
MSEO	Message start/end out	O	M	—

4 Electrical characteristics

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

4.1 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in Table 7 are used and the parameters are tagged accordingly in the tables where appropriate.

Table 7. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4.2 NVUSRO register

Bit values in the Non-Volatile User Options (NVUSRO) Register control portions of the device configuration, namely electrical parameters such as high voltage supply and oscillator margin, as well as digital functionality (watchdog enable/disable after reset). For a detailed description of the NVUSRO register, please refer to the device reference manual.

4.2.1 NVUSRO[PAD3V5V] field description

The DC electrical characteristics are dependent on the PAD3V5V bit value. Table 8 shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 8. PAD3V5V field description[1]

Value[2]	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1 See the device reference manual for more information on the NVUSRO register.

2 Default manufacturing value is ‘1’. Value can be programmed by customer in Shadow Flash.

4.2.2 NVUSRO[WATCHDOG_EN] field description

The watchdog enable/disable configuration after reset is dependent on the WATCHDOG_EN bit value. Table 10 shows how NVUSRO[WATCHDOG_EN] controls the device configuration.

Table 10. WATCHDOG_EN field description

Value[1]	Description
0	Disable after reset
1	Enable after reset

1 Default manufacturing value is '1'. Value can be programmed by customer in Shadow Flash.

4.3 Absolute maximum ratings

Table 11. Absolute maximum ratings

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	–0.3	6.0	V
V_{SS_LV}	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_BV}	SR	Voltage on VDD_BV (regulator supply) pin with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	–0.3	V_{DD} + 0.3	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pins with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_ADC}	SR	Voltage on VDD_HV_ADC0, VDD_HV_ADC1 (ADC reference) pins with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	V_{DD} − 0.3	V_{DD} + 0.3	

Table 11. Absolute maximum ratings (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	—	V_{DD} + 0.3	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
I_{AVGSEG}	SR	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	70	mA
			V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	64	
$T_{STORAGE}$	SR	Storage temperature	—	–55	150	°C

NOTE

Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

4.4 Recommended operating conditions

Table 12. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}[1]	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	3.0	3.6	V
V_{SS_LV}[2]	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS} − 0.1	V_{SS} + 0.1	V
V_{DD_BV}[3]	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	3.0	3.6	V
			Relative to V_{DD}	V_{DD} − 0.1	V_{DD} + 0.1	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS} − 0.1	V_{SS} + 0.1	V
V_{DD_ADC}[4]	SR	Voltage on VDD_HV_ADC0, VDD_HV_ADC1 (ADC reference) with respect to ground (V_{SS})	—	3.0[5]	3.6	V
			Relative to V_{DD}	V_{DD} − 0.1	V_{DD} + 0.1	

Table 12. Recommended operating conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	V_{SS} − 0.1	—	V
			Relative to V_{DD}	—	V_{DD}+ 0.1	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	−5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	−50	50	
TV_{DD}	SR	V_{DD} slope to ensure correct power up[6]	—	3.0[7]	0.25 V/µs	V/s
$T_{A\ C\text{-}Grade\ Part}$	SR	Ambient temperature under bias	$f_{CPU} \leq 64$ MHz[8]	−40	85	°C
$T_{J\ C\text{-}Grade\ Part}$	SR	Junction temperature under bias	—	−40	110	
$T_{A\ V\text{-}Grade\ Part}$	SR	Ambient temperature under bias	$f_{CPU} \leq 64$ MHz[8]	−40	105	
$T_{J\ V\text{-}Grade\ Part}$	SR	Junction temperature under bias	—	−40	130	
$T_{A\ M\text{-}Grade\ Part}$	SR	Ambient temperature under bias	$f_{CPU} \leq 64$ MHz[8]	−40	125	
$T_{J\ M\text{-}Grade\ Part}$	SR	Junction temperature under bias	—	−40	150	

1 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.

2 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.

3 470 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics). Supply ramp slope on VDD_BV should always be faster or equal to slope of VDD_HV. Otherwise, device may enter regulator bypass mode if slope on VDD_BV is slower.

4 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.

5 Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed. When voltage drops below V_{LVDHVL}, device is reset.

6 Guaranteed by device validation

7 Minimum value of TV_{DD} must be guaranteed until V_{DD} reaches 2.6 V (maximum value of V_{PORH})

8 When the FMPLL uses the frequency modulation with a modulation depth of 4% from the center spread frequency, the maximum value of f_{CPU} is 66.56 MHz.

Table 13. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}[1]	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop[2]	3.0	5.5	
V_{SS_LV}[3]	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS}− 0.1	V_{SS} + 0.1	V
V_{DD_BV}[4]	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop[2]	3.0	5.5	
			Relative to V_{DD}	3.0	V_{DD} + 0.1	

Table 13. Recommended operating conditions (5.0 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS} − 0.1	V_{SS} + 0.1	V
V_{DD_ADC}[5]	SR	Voltage on VDD_HV_ADC0, VDD_HV_ADC1 (ADC reference) with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop[2]	3.0	5.5	
			Relative to V_{DD}	V_{DD} − 0.1	V_{DD} + 0.1	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	V_{SS} − 0.1	—	V
			Relative to V_{DD}	—	V_{DD}+ 0.1	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	−5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	−50	50	
TV_{DD}	SR	V_{DD} slope to ensure correct power up[6]	—	3.0[7]	0.25 V/µs	V/s
$T_{A\ C\text{-}Grade\ Part}$	SR	Ambient temperature under bias	$f_{CPU} \leq 64$ MHz[8]	−40	85	°C
$T_{J\ C\text{-}Grade\ Part}$	SR	Junction temperature under bias	—	−40	110	
$T_{A\ V\text{-}Grade\ Part}$	SR	Ambient temperature under bias	$f_{CPU} \leq 64$ MHz[8]	−40	105	
$T_{J\ V\text{-}Grade\ Part}$	SR	Junction temperature under bias	—	−40	130	
$T_{A\ M\text{-}Grade\ Part}$	SR	Ambient temperature under bias	$f_{CPU} \leq 64$ MHz[8]	−40	125	
$T_{J\ M\text{-}Grade\ Part}$	SR	Junction temperature under bias	—	−40	150	

1 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.

2 Full device operation is guaranteed by design when the voltage drops below 4.5 V down to 3.0 V. However, certain analog electrical characteristics will not be guaranteed to stay within the stated limits.

3 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.

4 470 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics). While the supply voltage ramps up, the slope on V_{DD_BV} should be less than $0.9V_{DD\_HV}$ in order to ensure the device does not enter regulator bypass mode.

5 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.

6 Guaranteed by device validation

7 Minimum value of TV_{DD} must be guaranteed until V_{DD} reaches 2.6 V (maximum value of V_{PORH})

8 When the FMPLL uses the frequency modulation with a modulation depth of 4% from the center spread frequency, the maximum value of f_{CPU} is 66.56 MHz.

NOTE

RAM data retention is guaranteed with V_{DD_LV} not below 1.08 V.

4.5 Thermal characteristics

4.5.1 External ballast resistor recommendations

External ballast resistor on V_{DD_BV} pin helps in reducing the overall power dissipation inside the device. This resistor is required only when maximum power consumption exceeds the limit imposed by package thermal characteristics.

As stated in Table 14 LQFP thermal characteristics, considering a thermal resistance of 144 LQFP as 48.3 °C/W, at ambient temperature T_A = 125 °C, the junction temperature T_j will cross 150 °C if the total power dissipation is greater than (150 – 125)/48.3 = 517 mW. Therefore, the total device current I_{DDMAX} at 125 °C/5.5 V must not exceed 94.1 mA (i.e., PD/VDD). Assuming an average $I_{DD}(V_{DD\_HV})$ of 15–20 mA consumption typically during device RUN mode, the LV domain consumption $I_{DD}(V_{DD\_BV})$ is thus limited to $I_{DDMAX} - I_{DD}(V_{DD\_HV})$, i.e., 80 mA.

Therefore, respecting the maximum power allowed as explained in 4.5.2, Package thermal characteristics, it is recommended to use this resistor only in the 125 °C/5.5 V operating corner as per the following guidelines:

- If $I_{DD}(V_{DD\_BV}) < 80$ mA, then no resistor is required.
- If 80 mA < $I_{DD}(V_{DD\_BV}) < 90$ mA, then 4 Ω resistor can be used.
- If $I_{DD}(V_{DD\_BV}) > 90$ mA, then 8 Ω resistor can be used.

Using resistance in the range of 4–8 Ω, the gain will be around 10–20% of total consumption on V_{DD_BV}. For example, if 8 Ω resistor is used, then power consumption when $I_{DD}(V_{DD\_BV})$ is 110 mA is equivalent to power consumption when $I_{DD}(V_{DD\_BV})$ is 90 mA (approximately) when resistor not used.

In order to ensure correct power up, the minimum V_{DD_BV} to be guaranteed is 30 ms/V. If the supply ramp is slower than this value, then LVDHV3B monitoring ballast supply V_{DD_BV} pin gets triggered leading to device reset. Until the supply reaches certain threshold, this low voltage detector (LVD) generates destructive reset event in the system. This threshold depends on the maximum $I_{DD}(V_{DD\_BV})$ possible across the external resistor.

4.5.2 Package thermal characteristics

Table 14. LQFP thermal characteristics[1]

Symbol		C	Parameter	Conditions[2]	Pin count	Value			Unit
						Min	Typ	Max	
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection[3]	Single-layer board — 1s	100	—	—	64	°C/W
				Four-layer board — 2s2p	100	—	—	49.7	

Table 14. LQFP thermal characteristics[1] (continued)

Symbol		C	Parameter	Conditions[2]	Pin count	Value			Unit
						Min	Typ	Max	
$R_{\theta JB}$	CC		Thermal resistance, junction-to-board[4]	Single-layer board — 1s	100	—	—	36	°C/W
				Four-layer board — 2s2p	100	—	—	33.6	
$R_{\theta JC}$	CC		Thermal resistance, junction-to-case[5]	Single-layer board — 1s	100	—	—	23	°C/W
				Four-layer board — 2s2p	100	—	—	19.8	

1 Thermal characteristics are targets based on simulation.

2 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C.

3 Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package. When Greek letters are not available, the symbols are typed as R_{thJA} and R_{thJMA}.

4 Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. When Greek letters are not available, the symbols are typed as R_{thJB}.

5 Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer. When Greek letters are not available, the symbols are typed as R_{thJC}.

4.5.3 Power considerations

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using Equation 1:

$$T_J = T_A + (P_D \times R_{\theta JA}) \qquad \textit{Eqn. 1}$$

Where:

T_A is the ambient temperature in °C.

$R_{\theta JA}$ is the package junction-to-ambient thermal resistance, in °C/W.

P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$).

P_{INT} is the product of I_{DD} and V_{DD}, expressed in watts. This is the chip internal power.

$P_{I/O}$ represents the power dissipation on input and output pins; user determined.

Most of the time for the applications, $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant, if the device is configured to continuously drive external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273\ °C) \quad \textit{Eqn. 2}$$

Therefore, solving equations 1 and 2:

$$K = P_D \times (T_A + 273\ °C) + R_{\theta JA} \times P_D^2 \quad \textit{Eqn. 3}$$

Where:

K is a constant for the particular part, which may be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations 1 and 2 iteratively for any value of T_A.

4.6 I/O pad electrical characteristics

4.6.1 I/O pad types

The device provides four main I/O pad types depending on the associated alternate functions:

- Slow pads—are the most common pads, providing a good compromise between transition time and low electromagnetic emission.
- Medium pads—provide transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
- Fast pads—provide maximum speed. These are used for improved Nexus debugging capability.
- Input only pads—are associated with ADC channels and 32 kHz low power external crystal oscillator providing low input leakage.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance.

4.6.2 I/O input DC characteristics

Table 15 provides input DC electrical characteristics as described in Figure 8.

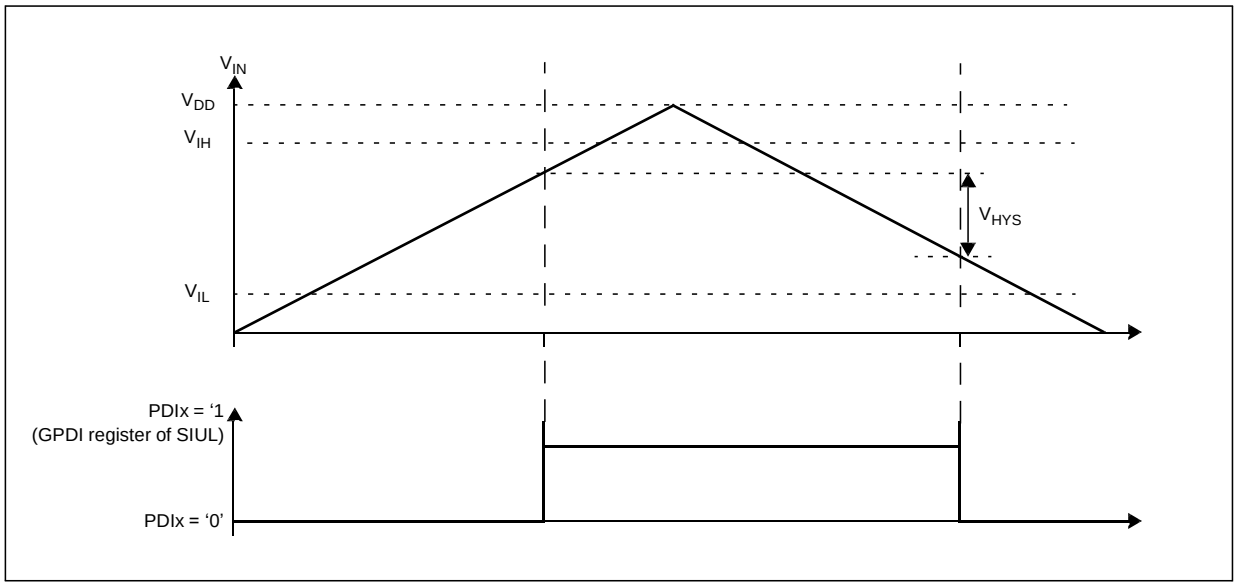


Figure 8. I/O input DC electrical characteristics definition

Table 15. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	—		$0.65V_{DD}$	—	V_{DD} + 0.4	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	—		−0.4	—	$0.35V_{DD}$	
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—		$0.1V_{DD}$	—	—	
I_{LKG}	CC	D	Digital input leakage	No injection on adjacent pin	T_A = −40 °C	—	2	200	nA
		D			T_A = 25 °C	—	2	200	
		D			T_A = 85 °C	—	5	300	
		D			T_A = 105 °C	—	12	500	
		P			T_A = 125 °C	—	70	1000	
W_{FI}[2]	SR	P	Wakeup input filtered pulse	—		—	—	40	ns
W_{NFI}[2]	SR	P	Wakeup input not filtered pulse	—		1000	—	—	ns

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified

2 In the range from 40 to 1000 ns, pulses can be filtered or not filtered, according to operating temperature and voltage.

4.6.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- Table 16 provides weak pull figures. Both pull-up and pull-down resistances are supported.

- Table 17 provides output driver characteristics for I/O pads when in SLOW configuration.
- Table 18 provides output driver characteristics for I/O pads when in MEDIUM configuration.
- Table 19 provides output driver characteristics for I/O pads when in FAST configuration.

Table 16. I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
$\|I_{WPU}\|$	CC	P	Weak pull-up current absolute value	$V_{IN} = V_{IL}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1[2]	10	—	250	
		P		$V_{IN} = V_{IL}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	
$\|I_{WPD}\|$	CC	P	Weak pull-down current absolute value	$V_{IN} = V_{IH}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1	10	—	250	
		P		$V_{IN} = V_{IH}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified.

2 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 17. SLOW configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level SLOW configuration	Push Pull	I_{OH} = −2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	0.8V_{DD}	—	—	V
		C			I_{OH} = −2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	0.8V_{DD}	—	—	
		C			I_{OH} = −1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} − 0.8	—	—	
V_{OL}	CC	P	Output low level SLOW configuration	Push Pull	I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	0.1V_{DD}	V
		C			I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	0.1V_{DD}	
		C			I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified

[2] The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 18. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	C	Output high level MEDIUM configuration	Push Pull	I_{OH} = −3.8 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	V
		P			I_{OH} = −2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	
		C			I_{OH} = −1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C			I_{OH} = −1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} − 0.8	—	—	
		C			I_{OH} = −100 µA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	
V_{OL}	CC	C	Output low level MEDIUM configuration	Push Pull	I_{OL} = 3.8 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.2V_{DD}$	V
		P			I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
		C			I_{OL} = 100 µA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.1V_{DD}$	

[1] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified

[2] The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 19. FAST configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level FAST configuration	Push Pull	I_{OH} = −14 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	V
		C			I_{OH} = −7 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C			I_{OH} = −11 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} − 0.8	—	—	
V_{OL}	CC	P	Output low level FAST configuration	Push Pull	I_{OL} = 14 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 7 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C			I_{OL} = 11 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified

2 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

4.6.4 Output pin transition times

Table 20. Output pin transition times

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
t_{tr}	CC	D	Output transition time output pin[2] SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	

Table 20. Output pin transition times (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
t_{tr}	CC	D	Output transition time output pin[2] MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C_L = 50 pF		—	—	20	
		D		C_L = 100 pF		—	—	40	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C_L = 50 pF		—	—	25	
		D		C_L = 100 pF		—	—	40	
t_{tr}	CC	D	Output transition time output pin[2] FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	4	ns
				C_L = 50 pF		—	—	6	
				C_L = 100 pF		—	—	12	
				C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	4	
				C_L = 50 pF		—	—	7	
				C_L = 100 pF		—	—	12	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified

2 C_L includes device and package capacitances (C_{PKG} < 5 pF).

4.6.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in Table 21.

Table 22 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

Table 21. I/O supply segments

Package	Supply segment							
	1	2	3	4	5	6	7	8
100 LQFP	pin16 – pin35	pin37 – pin69	pin70 – pin83	pin84 – pin15	—	—	—	—

Table 22. I/O consumption

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{SWTSLW}[2]	CC	D	Dynamic I/O current for SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16	
I_{SWTMED}[2]	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	29	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	17	
I_{SWTFST}[2]	CC	D	Dynamic I/O current for FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	110	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
I_{RMSSLW}	CC	D	Root mean square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.3	mA
				C_L = 25 pF, 4 MHz		—	—	3.2	
				C_L = 100 pF, 2 MHz		—	—	6.6	
				C_L = 25 pF, 2 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.6	
				C_L = 25 pF, 4 MHz		—	—	2.3	
				C_L = 100 pF, 2 MHz		—	—	4.7	
I_{RMSMED}	CC	D	Root mean square I/O current for MEDIUM configuration	C_L = 25 pF, 13 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.6	mA
				C_L = 25 pF, 40 MHz		—	—	13.4	
				C_L = 100 pF, 13 MHz		—	—	18.3	
				C_L = 25 pF, 13 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	5	
				C_L = 25 pF, 40 MHz		—	—	8.5	
				C_L = 100 pF, 13 MHz		—	—	11	
I_{RMSFST}	CC	D	Root mean square I/O current for FAST configuration	C_L = 25 pF, 40 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	22	mA
				C_L = 25 pF, 64 MHz		—	—	33	
				C_L = 100 pF, 40 MHz		—	—	56	
				C_L = 25 pF, 40 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14	
				C_L = 25 pF, 64 MHz		—	—	20	
				C_L = 100 pF, 40 MHz		—	—	35	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to125 °C, unless otherwise specified

2 Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

Table 23 provides the weight of concurrent switching I/Os.

Due to the dynamic current limitations, the sum of the weight of concurrent switching I/Os on a single segment must not exceed 100% to ensure device functionality.

Table 23. I/O weight[1]

Supply segment		Pad	100 LQFP			
			Weight 5 V		Weight 3.3 V	
	100 LQFP		SRC = 0	SRC = 1	SRC = 0	SRC = 1
	4	PB[3]	13%	—	15%	—
		PC[9]	13%	—	15%	—
		PC[14]	13%	—	15%	—
		PC[15]	12%	18%	15%	16%
	—	PJ[4]	—	—	—	—
	—	PH[15]	—	—	—	—
	—	PH[13]	—	—	—	—
	—	PH[14]	—	—	—	—
	—	PI[6]	—	—	—	—
	—	PI[7]	—	—	—	—
	—	PG[5]	—	—	—	—
	—	PG[4]	—	—	—	—
	—	PG[3]	—	—	—	—
	—	PG[2]	—	—	—	—
	4	PA[2]	8%	—	10%	—
		PE[0]	8%	—	9%	—
		PA[1]	8%	—	9%	—
		PE[1]	7%	10%	9%	9%
		PE[8]	7%	10%	8%	9%
		PE[9]	6%	—	8%	—
		PE[10]	6%	—	7%	—
		PA[0]	6%	8%	7%	7%
		PE[11]	5%	—	6%	—

Table 23. I/O weight[1] (continued)

Supply segment		Pad	100 LQFP			
			Weight 5 V		Weight 3.3 V	
	100 LQFP		SRC = 0	SRC = 1	SRC = 0	SRC = 1
	—	PG[9]	—	—	—	—
	—	PG[8]	—	—	—	—
	1	PC[11]	9%	—	11%	—
		PC[10]	9%	13%	11%	12%
	—	PG[7]	—	—	—	—
	—	PG[6]	—	—	—	—
	1	PB[0]	10%	14%	12%	12%
		PB[1]	10%	—	12%	—
	—	PF[9]	—	—	—	—
	—	PF[8]	—	—	—	—
	—	PF[12]	—	—	—	—
	1	PC[6]	—	—	—	—
		PC[7]	10%	—	12%	—
	—	PF[10]	—	—	—	—
	—	PF[11]	—	—	—	—
	1	PA[15]	8%	12%	10%	10%
	—	PF[13]	—	—	—	—
	1	PA[14]	8%	11%	9%	10%
		PA[4]	7%	—	9%	—
		PA[13]	7%	10%	8%	9%
		PA[12]	7%	—	8%	—

Table 23. I/O weight[1] (continued)

Supply segment		Pad	100 LQFP			
			Weight 5 V		Weight 3.3 V	
	100 LQFP		SRC = 0	SRC = 1	SRC = 0	SRC = 1
	2	PB[9]	1%	—	1%	—
		PB[8]	1%	—	1%	—
		PB[10]	6%	—	7%	—
	—	PF[0]	—	—	—	—
	—	PF[1]	—	—	—	—
	—	PF[2]	—	—	—	—
	—	PF[3]	—	—	—	—
	—	PF[4]	—	—	—	—
	—	PF[5]	—	—	—	—
	—	PF[6]	—	—	—	—
	—	PF[7]	—	—	—	—
	—	PJ[3]	—	—	—	—
	—	PJ[2]	—	—	—	—
	—	PJ[1]	—	—	—	—
	—	PJ[0]	—	—	—	—
	—	PI[15]	—	—	—	—
	—	PI[14]	—	—	—	—
	2	PD[0]	1%	—	1%	—
		PD[1]	1%	—	1%	—
		PD[2]	1%	—	1%	—
		PD[3]	1%	—	1%	—
		PD[4]	1%	—	1%	—
		PD[5]	1%	—	1%	—
		PD[6]	1%	—	2%	—
		PD[7]	1%	—	2%	—

Table 23. I/O weight[1] (continued)

Supply segment		Pad	100 LQFP			
			Weight 5 V		Weight 3.3 V	
	100 LQFP		SRC = 0	SRC = 1	SRC = 0	SRC = 1
	2	PD[8]	1%	—	2%	—
		PB[4]	1%	—	2%	—
		PB[5]	1%	—	2%	—
		PB[6]	1%	—	2%	—
		PB[7]	1%	—	2%	—
		PD[9]	1%	—	2%	—
		PD[10]	1%	—	2%	—
		PD[11]	1%	—	2%	—
	—	PB[11]	—	—	—	—
	—	PD[12]	—	—	—	—
	2	PB[12]	15%	—	17%	—
		PD[13]	14%	—	17%	—
		PB[13]	14%	—	17%	—
		PD[14]	14%	—	17%	—
		PB[14]	14%	—	16%	—
		PD[15]	13%	—	16%	—
		PB[15]	13%	—	15%	—
	—	PI[8]	—	—	—	—
	—	PI[9]	—	—	—	—
	—	PI[10]	—	—	—	—
	—	PI[11]	—	—	—	—
	—	PI[12]	—	—	—	—
	—	PI[13]	—	—	—	—
	2	PA[3]	11%	—	13%	—
	—	PG[13]	—	—	—	—
	—	PG[12]	—	—	—	—
	—	PH[0]	—	—	—	—
	—	PH[1]	—	—	—	—
	—	PH[2]	—	—	—	—
	—	PH[3]	—	—	—	—
	—	PG[1]	—	—	—	—
	—	PG[0]	—	—	—	—

Table 23. I/O weight[1] (continued)

Supply segment		Pad	100 LQFP			
			Weight 5 V		Weight 3.3 V	
	100 LQFP		SRC = 0	SRC = 1	SRC = 0	SRC = 1
	—	PF[15]	—	—	—	—
	—	PF[14]	—	—	—	—
	—	PE[13]	4%	—	5%	—
	3	PA[7]	5%	—	6%	—
		PA[8]	5%	—	6%	—
		PA[9]	6%	—	7%	—
		PA[10]	6%	—	8%	—
		PA[11]	8%	—	9%	—
		PE[12]	8%	—	9%	—
	—	PG[14]	—	—	—	—
	—	PG[15]	—	—	—	—
	—	PE[14]	8%	—	9%	—
	—	PE[15]	8%	11%	9%	10%
	—	PG[10]	—	—	—	—
	—	PG[11]	—	—	—	—
	—	PH[11]	—	—	—	—
	—	PH[12]	—	—	—	—
	—	PI[5]	—	—	—	—
	—	PI[4]	—	—	—	—
	3	PC[3]	6%	—	8%	—
		PC[2]	6%	8%	7%	7%
		PA[5]	6%	8%	7%	7%
		PA[6]	5%	—	6%	—
		PH[10]	—	—	—	—
		PC[1]	5%	19%	5%	13%

Table 23. I/O weight[1] (continued)

Supply segment		Pad	100 LQFP			
			Weight 5 V		Weight 3.3 V	
	100 LQFP		SRC = 0	SRC = 1	SRC = 0	SRC = 1
	4	PC[0]	7%	10%	8%	8%
		PH[9]	—	—	—	—
		PE[2]	8%	11%	9%	10%
		PE[3]	8%	12%	10%	10%
		PC[5]	8%	12%	10%	11%
		PC[4]	9%	13%	10%	11%
		PE[4]	9%	13%	11%	12%
		PE[5]	9%	14%	11%	12%
	—	PH[4]	—	—	—	—
	—	PH[5]	—	—	—	—
	—	PH[6]	—	—	—	—
	—	PH[7]	—	—	—	—
	—	PH[8]	—	—	—	—
	4	PE[6]	11%	16%	13%	14%
		PE[7]	11%	16%	14%	14%
	—	PI[3]	—	—	—	—
	—	PI[2]	—	—	—	—
	—	PI[1]	—	—	—	—
	—	PI[0]	—	—	—	—
	4	PC[12]	12%	18%	15%	16%
		PC[13]	13%	—	15%	—
		PC[8]	13%	—	15%	—
		PB[2]	13%	18%	15%	16%

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified
2 SRC: “Slew Rate Control” bit in SIU_PCRx

4.6.6 $\overline{\text{RESET}}$ electrical characteristics

The device implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

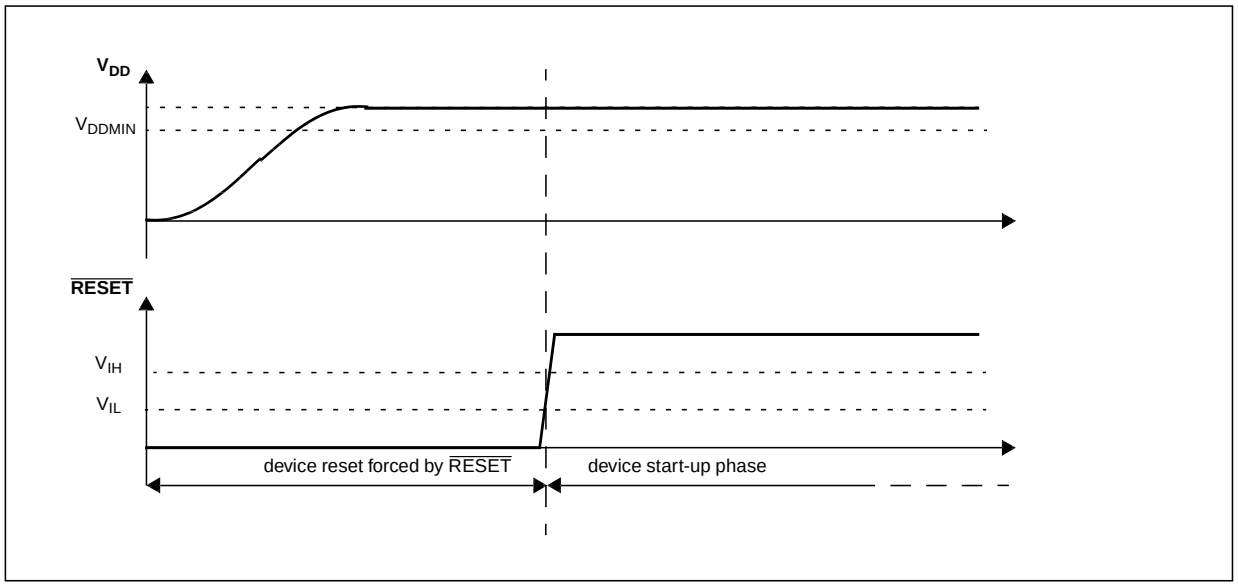


Figure 9.1. Start-up reset requirements

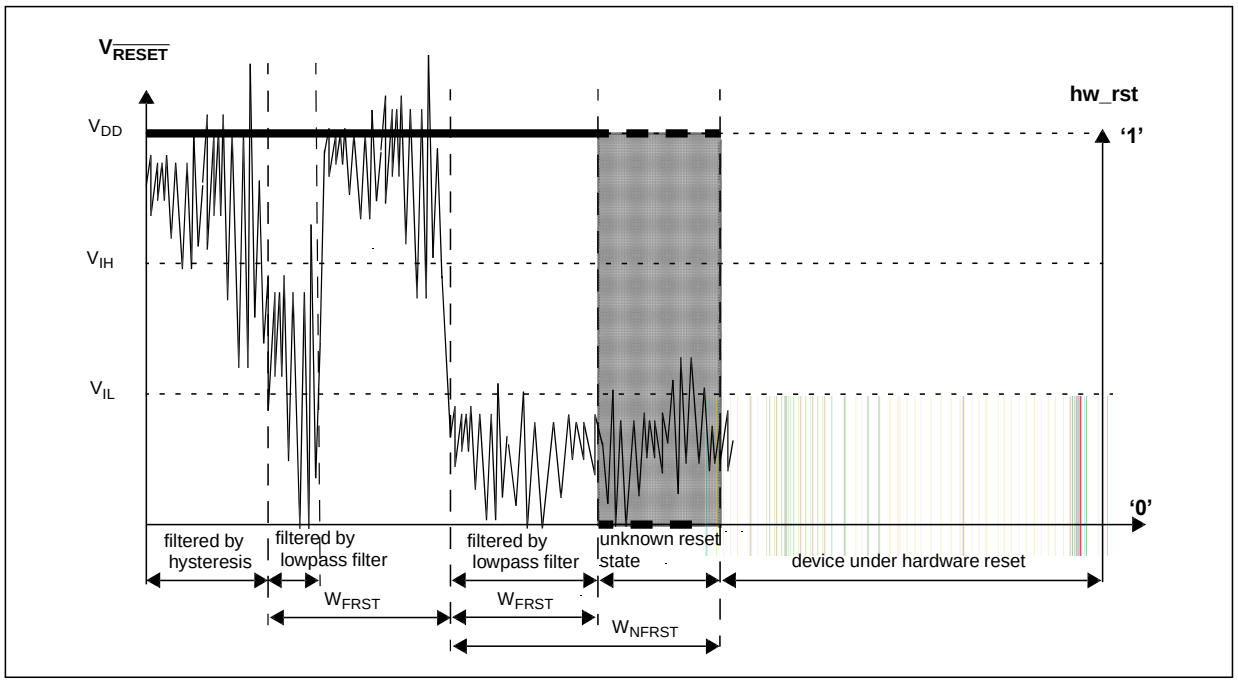


Figure 9.2. Noise filtering on reset signal

Table 24. Reset electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input High Level CMOS (Schmitt Trigger)	—	$0.65V_{DD}$	—	V_{DD} + 0.4	V

Table 24. Reset electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{IL}	SR	P	Input low Level CMOS (Schmitt Trigger)	—	−0.4	—	$0.35V_{DD}$	V
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—	$0.1V_{DD}$	—	—	V
V_{OL}	CC	P	Output low level	Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
				Push Pull, I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
				Push Pull, I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
t_{tr}	CC	D	Output transition time output pin[3] MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
				C_L = 100 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
				C_L = 100 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
W_{FRST}	SR	P	RESET input filtered pulse	—	—	—	40	ns
W_{NFRST}	SR	P	RESET input not filtered pulse	—	1000	—	—	ns
$\|I_{WPU}\|$	CC	P	Weak pull-up current absolute value	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	10	—	150	µA
		D		V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	10	—	150	
		P		V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[4]	10	—	250	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified

2 This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to RGM module section of the device reference manual).

3 C_L includes device and package capacitance (C_{PKG} < 5 pF).

4 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

4.7 Power management electrical characteristics

4.7.1 Voltage regulator electrical characteristics

The device implements an internal voltage regulator to generate the low voltage core supply V_{DD_LV} from the high voltage ballast supply V_{DD_BV}. The regulator itself is supplied by the common I/O supply V_{DD}. The following supplies are involved:

- HV: High voltage external power supply for voltage regulator module. This must be provided externally through V_{DD} power pin.
- BV: High voltage external power supply for internal ballast module. This must be provided externally through V_{DD_BV} power pin. Voltage values should be aligned with V_{DD}.
- LV: Low voltage internal power supply for core, FMPLL and Flash digital logic. This is generated by the internal voltage regulator but provided outside to connect stability capacitor. It is further split into four main domains to ensure noise isolation between critical LV modules within the device:
  - LV_COR: Low voltage supply for the core. It is also used to provide supply for FMPLL through double bonding.
  - LV_CFLA: Low voltage supply for code flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
  - LV_DFLA: Low voltage supply for data flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
  - LV_PLL: Low voltage supply for FMPLL. It is shorted to LV_COR through double bonding.

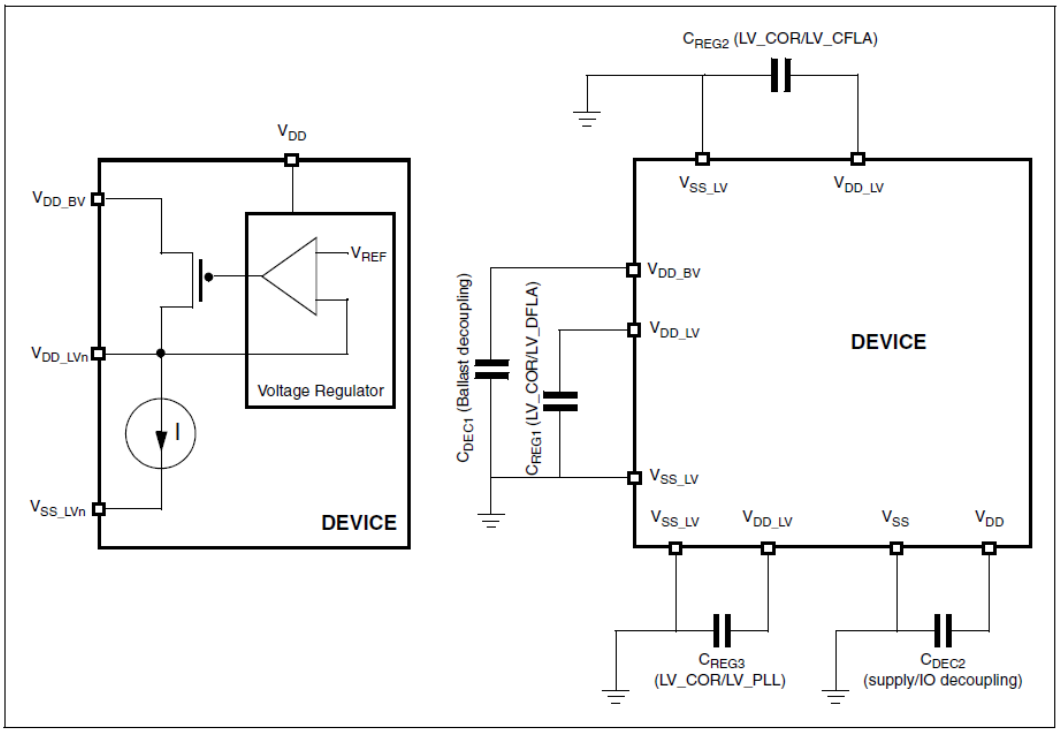


Figure 10. Voltage regulator capacitance connection

The internal voltage regulator requires external capacitance (C_{REGn}) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 5 nH.

Each decoupling capacitor must be placed between each of the three V_{DD_LV}/V_{SS_LV} supply pairs to ensure stable voltage (see 4.4, Recommended operating conditions).

Table 25. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
C_{REGn}	SR	—	Internal voltage regulator external capacitance	—	200	—	500	nF
R_{REG}	SR	—	Stability capacitor equivalent serial resistance	Range: 10 kHz to 20 MHz	—	—	0.2	Ω
C_{DEC1}	SR	—	Decoupling capacitance[2] ballast	V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 4.5 V to 5.5 V	100[3]	470[4]	—	nF
				V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 3 V to 3.6 V	400		—	

Table 25. Voltage regulator electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
C_{DEC2}	SR	—	Decoupling capacitance regulator supply	V_{DD}/V_{SS} pair	10	100	—	nF
V_{MREG}	CC	T	Main regulator output voltage	Before exiting from reset	—	1.32	—	V
		P		After trimming	1.16	1.28	—	
I_{MREG}	SR	—	Main regulator current provided to V_{DD_LV} domain	—	—	—	150	mA
$I_{MREGINT}$	CC	D	Main regulator module current consumption	I_{MREG} = 200 mA	—	—	2	mA
				I_{MREG} = 0 mA	—	—	1	
V_{LPREG}	CC	P	Low-power regulator output voltage	After trimming	1.16	1.28	—	V
I_{LPREG}	SR	—	Low-power regulator current provided to V_{DD_LV} domain	—	—	—	15	mA
$I_{LPREGINT}$	CC	D	Low-power regulator module current consumption	I_{LPREG} = 15 mA; T_A = 55 °C	—	—	600	µA
		—		I_{LPREG} = 0 mA; T_A = 55 °C	—	5	—	
V_{ULPREG}	CC	P	Ultra low power regulator output voltage	After trimming	1.16	1.28	—	V
I_{ULPREG}	SR	—	Ultra low power regulator current provided to V_{DD_LV} domain	—	—	—	5	mA
$I_{ULPREGINT}$	CC	D	Ultra low power regulator module current consumption	I_{ULPREG} = 5 mA; T_A = 55 °C	—	—	100	µA
				I_{ULPREG} = 0 mA; T_A = 55 °C	—	2	—	
I_{DD_BV}	CC	D	In-rush average current on V_{DD_BV} during power-up[5]	—	—	—	300[6]	mA

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified

2 This capacitance value is driven by the constraints of the external voltage regulator supplying the V_{DD_BV} voltage. A typical value is in the range of 470 nF.

3 This value is acceptable to guarantee operation from 4.5 V to 5.5 V

4 External regulator and capacitance circuitry must be capable of providing I_{DD_BV} while maintaining supply V_{DD_BV} in operating range.

5 In-rush average current is seen only for short time during power-up and on standby exit (maximum 20 µs, depending on external capacitances to be loaded).

6 The duration of the in-rush current depends on the capacitance placed on LV pins. BV decoupling capacitors must be sized accordingly. Refer to I_{MREG} value for minimum amount of current to be provided in cc.

4.7.2 Low voltage detector electrical characteristics

The device implements a power-on reset (POR) module to ensure correct power-up initialization, as well as five low voltage detectors (LVDs) to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state (refer to RGM Destructive Event Status (RGM_DES) Register flag F_POR in device reference manual)
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD27 in device reference manual)
- LVDHV3B monitors V_{DD_BV} to ensure device reset below minimum functional supply (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD27_VREG in device reference manual)
- LVDHV5 monitors V_{DD} when application uses device in the 5.0 V ± 10% range (refer to RGM Functional Event Status (RGM_FES) Register flag F_LVD45 in device reference manual)
- LVDLVCOR monitors power domain No. 1 (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD12_PD1 in device reference manual)
- LVDLVBKP monitors power domain No. 0 (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD12_PD0 in device reference manual)

NOTE

When enabled, power domain No. 2 is monitored through LVDLVBKP.

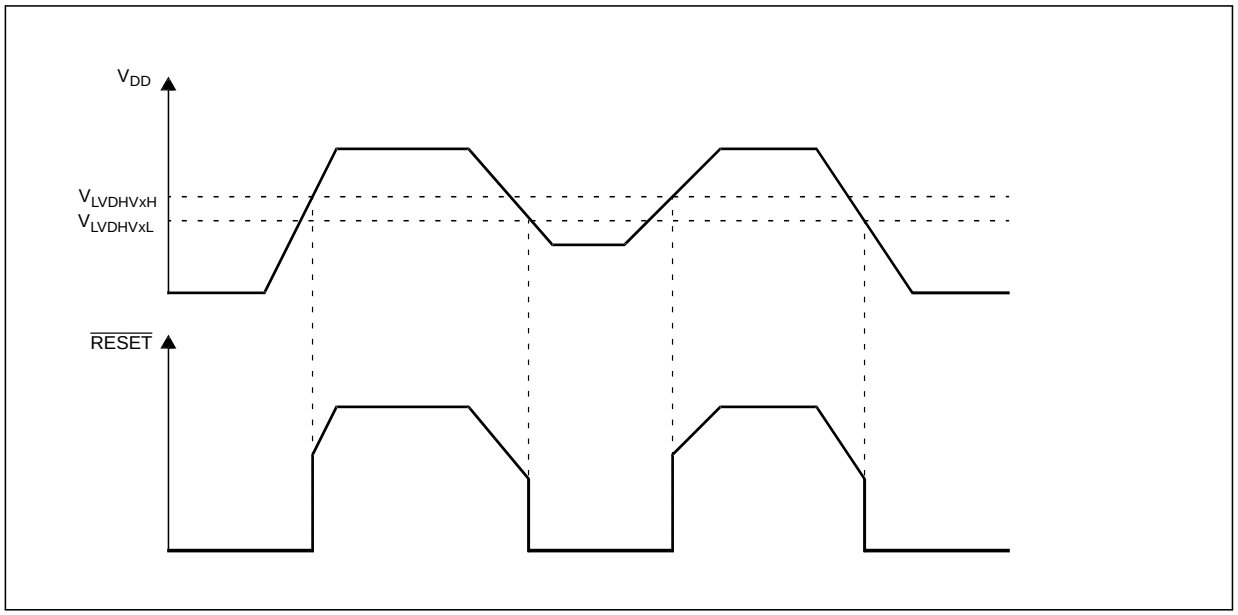


Figure 11. Low voltage detector vs reset

Table 26. Low voltage detector electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{PORUP}	SR	P	Supply for functional POR module	T_A = 25 °C, after trimming	1.0	—	5.5	V
V_{PORH}	CC	P	Power-on reset threshold		1.5	—	2.6	
$V_{LVDHV3H}$	CC	T	LVDHV3 low voltage detector high threshold		—	—	2.95	
$V_{LVDHV3L}$	CC	P	LVDHV3 low voltage detector low threshold		2.6	—	2.9	
$V_{LVDHV3BH}$	CC	P	LVDHV3B low voltage detector high threshold		—	—	2.95	
$V_{LVDHV3BL}$	CC	P	LVDHV3B low voltage detector low threshold		2.6	—	2.9	
$V_{LVDHV5H}$	CC	T	LVDHV5 low voltage detector high threshold		—	—	4.5	
$V_{LVDHV5L}$	CC	P	LVDHV5 low voltage detector low threshold		3.8	—	4.4	
$V_{LVDLVCORL}$	CC	P	LVDLVCOR low voltage detector low threshold		1.08	—	1.16	
$V_{LVDLVBKPL}$	CC	P	LVDLVBKP low voltage detector low threshold		1.08	—	1.16	

[1] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified

4.8 Power consumption

Table 27 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

Table 27. Power consumption on VDD_BV and VDD_HV

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{DDMAX}[2]	CC	D	RUN mode maximum average current	—		—	115	140[3]	mA
I_{DDRUN}[4]	CC	T	RUN mode typical average current[5]	f_{CPU} = 8 MHz		—	12	—	mA
		T		f_{CPU} = 16 MHz		—	27	—	
		T		f_{CPU} = 32 MHz		—	43	—	
		P		f_{CPU} = 48 MHz		—	56	100	
		P		f_{CPU} = 64 MHz		—	70	125	
I_{DDHALT}	CC	C	HALT mode current[6]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	10	18	mA
		P			T_A = 125 °C	—	17	28	
I_{DDSTOP}	CC	P	STOP mode current[7]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	350	900[8]	µA
		D			T_A = 55 °C	—	750	—	
		D			T_A = 85 °C	—	2	7	mA
		D			T_A = 105 °C	—	4	10	
		P			T_A = 125 °C	—	7	14	

Table 27. Power consumption on VDD_BV and VDD_HV (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
$I_{DDSTDBY2}$	CC	P	STANDBY2 mode current[9]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	30	100	µA
		D			T_A = 55 °C	—	75	—	
		D			T_A = 85 °C	—	180	700	
		D			T_A = 105 °C	—	315	1000	
		P			T_A = 125 °C	—	560	1700	
$I_{DDSTDBY1}$	CC	T	STANDBY1 mode current[10]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	20	60	µA
		D			T_A = 55 °C	—	45	—	
		D			T_A = 85 °C	—	100	350	
		D			T_A = 105 °C	—	165	500	
		D			T_A = 125 °C	—	280	900	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified

2 Running consumption does not include I/Os toggling which is highly dependent on the application. The given value is thought to be a worst case value with all peripherals running, and code fetched from code flash while modify operation ongoing on data flash. Notice that this value can be significantly reduced by application: switch off not used peripherals (default), reduce peripheral frequency through internal prescaler, fetch from RAM most used functions, use low power mode when possible.

3 Higher current may be sunk by device during power-up and standby exit. Please refer to in-rush average current in Table 25.

4 RUN current measured with typical application with accesses on both Flash and RAM.

5 Only for the “P” classification: Data and Code Flash in Normal Power. Code fetched from RAM: Serial IPs CAN and LIN in loop back mode, DSPI as Master, PLL as system clock (4 x Multiplier) peripherals on (eMIOS/CTU/ADC) and running at max frequency, periodic SW/WDG timer reset enabled.

6 Data Flash Power Down. Code Flash in Low Power. SIRC 128 kHz and FIRC 16 MHz on. 10 MHz XTAL clock. FlexCAN: instances: 0, 1, 2 ON (clocked but not reception or transmission), instances: 4, 5, 6 clocks gated. LINFlex: instances: 0, 1, 2 ON (clocked but not reception or transmission), instance: 3 to 9 clocks gated. eMIOS: instance: 0 ON (16 channels on PA[0]–PA[11] and PC[12]–PC[15]) with PWM 20 kHz, instance: 1 clock gated. DSPI: instance: 0 (clocked but no communication), instance: 1 to 5 clocks gated. RTC/API ON. PIT ON. STM ON. ADC1 OFF. ADC0 ON but no conversion except two analog watchdogs.

7 Only for the “P” classification: No clock, FIRC 16 MHz off, SIRC 128 kHz on, PLL off, HPvreg off, ULPVreg/LPVreg on. All possible peripherals off and clock gated. Flash in power down mode.

8 When going from RUN to STOP mode and the core consumption is > 6 mA, it is normal operation for the main regulator module to be kept on by the on-chip current monitoring circuit. This is most likely to occur with junction temperatures exceeding 125 °C and under these circumstances, it is possible for the current to initially exceed the maximum STOP specification by up to 2 mA. After entering stop, the application junction temperature will reduce to the ambient level and the main regulator will be automatically switched off when the load current is below 6 mA.

9 Only for the “P” classification: ULPreg on, HP/LPVreg off, 32 KB RAM on, device configured for minimum consumption, all possible modules switched off.

10 ULPreg on, HP/LPVreg off, 8 KB RAM on, device configured for minimum consumption, all possible modules switched off.

4.9 Flash memory electrical characteristics

4.9.1 Program/erase characteristics

Table 28 shows the program and erase characteristics.

Table 28. Program and erase specifications

Symbol		C	Parameter	Conditions	Value				Unit
					Min	Typ[1]	Initial max[2]	Max[3]	
$t_{dwprogram}$	CC	C	Double word (64 bits) program time[4]	Code Flash	—	18	50	500	µs
				Data Flash		22			
$t_{16Kpperase}$			16 KB block preprogram and erase time	Code Flash	—	200	500	5000	ms
				Data Flash		300			
$t_{32Kpperase}$			32 KB block preprogram and erase time	Code Flash	—	300	600	5000	ms
				Data Flash		400			
$t_{128Kpperase}$			128 KB block preprogram and erase time	Code Flash	—	600	1300	7500	ms
				Data Flash		800			
t_{esus}		D	Erase Suspend Latency	—	—	—	30	30	µs
t_{ESRT}		C	Erase Suspend Request Rate[5]	Code Flash	20	—	—	—	ms
				Data Flash	10	—	—	—	

1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3 The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

5 Time between erase suspend resume and the next erase suspend request

Table 29. Flash module life

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
P/E	CC	C	—	Code Flash	100,000	—	—	cycles
				Data Flash	100,000		—	
Retention	CC	C	Minimum data retention at 85 °C average ambient temperature[1]	Blocks with 0–1,000 P/E cycles	20	—	—	years
				Blocks with 1,001–10,000 P/E cycles	10	—	—	years
				Blocks with 10,001–100,000 P/E cycles	5	—	—	years

1 Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 30. Flash read access timing

Symbol		C	Parameter	Conditions[1]	Max	Unit
f_{READ}	CC	P	Maximum frequency for Flash reading	2 wait states	64	MHz
		C		2 wait state	40	
		C		2 wait states	20	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified

4.9.2 Flash power supply DC characteristics

Table 31 shows the power supply DC characteristics on external supply.

Table 31. Flash power supply DC electrical characteristics

Symbol		Parameter	Conditions[1]		Value			Unit
					Min	Typ	Max	
I_{CFREAD}	CC	Sum of the current consumption on V_{DD_HV} and V_{DD_BV} on read access	Flash module read f_{CPU} = 64 MHz	Code Flash	—	—	33	mA
I_{DFREAD}				Data Flash	—	—	33	
I_{CFMOD}	CC	Sum of the current consumption on V_{DD_HV} and V_{DD_BV} on matrix modification (program/erase)	Program/Erase on-going while reading Flash registers f_{CPU} = 64 MHz	Code Flash	—	—	52	mA
I_{DFMOD}				Data Flash	—	—	33	
I_{CFLPW}	CC	Sum of the current consumption on V_{DD_HV} and V_{DD_BV} during Flash low power mode	—	Code Flash	—	—	1.1	mA
I_{DFLPW}				Data Flash	—	—	900	µA
I_{CFPWD}	CC	Sum of the current consumption on V_{DD_HV} and V_{DD_BV} during Flash power down mode	—	Code Flash	—	—	150	µA
I_{DFPWD}				Data Flash	—	—	150	

[1] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

4.9.3 Start-up/Switch-off timings

Table 32. Start-up time/Switch-off time

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
$t_{FLARSTEXIT}$	CC	T	Delay for Flash module to exit reset mode	—	—	—	125	µs
$t_{FLALPEXIT}$	CC	T	Delay for Flash module to exit low-power mode	—	—	—	0.5	
$t_{FLAPDEXIT}$	CC	T	Delay for Flash module to exit power-down mode	—	—	—	30	
$t_{FLALPENTRY}$	CC	T	Delay for Flash module to enter low-power mode	—	—	—	0.5	
$t_{FLAPDENTRY}$	CC	T	Delay for Flash module to enter power-down mode	—	—	—	1.5	

[1] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified

4.10 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

4.10.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and prequalification tests in relation with the EMC level requested for the application.

- Software recommendations − The software flowchart must include the management of runaway conditions such as:
  - — Corrupted program counter
  - — Unexpected reset
  - — Critical data corruption (control registers...)
- Prequalification trials − Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

  To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

4.10.2 Electromagnetic interference (EMI)

The product is monitored in terms of emission based on a typical application. This emission test conforms to the IEC61967-1 standard, which specifies the general conditions for EMI measurements.

Table 33. EMI radiated emission measurement[1,2]

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
—	SR	—	Scan range	—		0.150		1000	MHz
f_{CPU}	SR	—	Operating frequency	—		—	64	—	MHz
V_{DD_LV}	SR	—	LV operating voltages	—		—	1.28	—	V
S_{EMI}	CC	T	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP144 package Test conforming to IEC 61967-2, f_{OSC} = 8 MHz/f_{CPU} = 64 MHz	No PLL frequency modulation	—	—	18	dBµV
					± 2% PLL frequency modulation	—	—	14	dBµV

1 EMI testing and I/O port waveforms per IEC 61967-1, -2, -4

2 For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.

4.10.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

4.10.3.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts×(n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

Table 34. ESD absolute maximum ratings[1,2]

Symbol	Ratings	Conditions	Class	Max value[3]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500	
				750 (corners)	

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3 Data based on characterization results, not tested in production

4.10.3.2 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 35. Latch-up results

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

4.11 Fast external crystal oscillator (4 to 20 MHz) electrical characteristics

The device provides an oscillator/resonator driver. Figure 12 describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

Table 36 provides the parameter description of 4 MHz to 20 MHz crystals used for the design simulations.

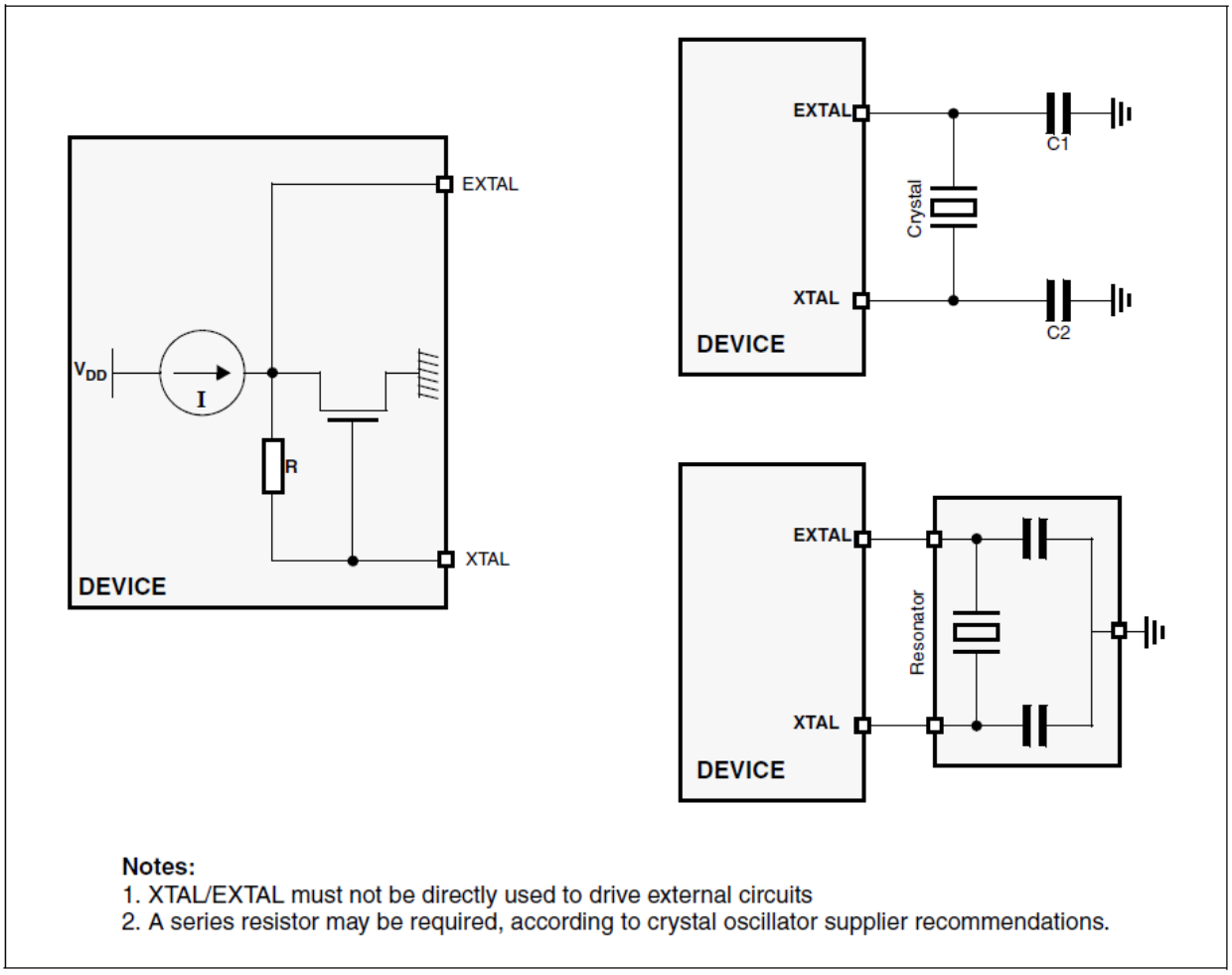


Figure 12. Crystal oscillator and resonator connection scheme

Table 36. Crystal description

Nominal frequency (MHz)	NDK crystal reference	Crystal equivalent series resistance ESR Ω	Crystal motional capacitance (C_m) fF	Crystal motional inductance (L_m) mH	Load on xtalin/xtalout C1 = C2 (pF)[1]	Shunt capacitance between xtalout and xtalin C0[2] (pF)
4	NX8045GB	300	2.68	591.0	21	2.93
8	NX5032GA	300	2.46	160.7	17	3.01
10		150	2.93	86.6	15	2.91
12		120	3.11	56.5	15	2.93
16		120	3.90	25.3	10	3.00
20		120	3.95	18.5	10	3.00

1 The values specified for C1 and C2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.

2 The value of C0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

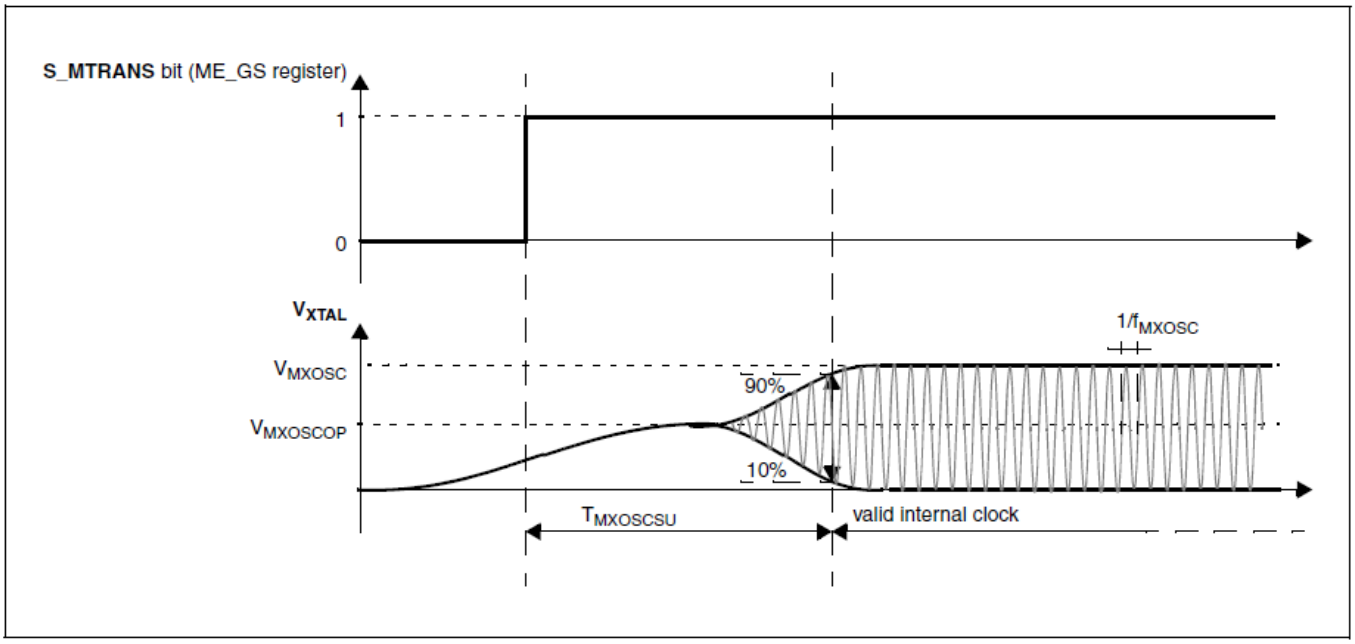


Figure 13. Fast external crystal oscillator (4 to 20 MHz) timing diagram

Table 37. Fast external crystal oscillator (4 to 20 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{FXOSC}	SR	—	Fast external crystal oscillator frequency	—	4.0	—	20.0[3]	MHz
g_{mFXOSC}	CC	C	Fast external crystal oscillator transconductance	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 0	2.2	—	8.2	mA/V
	CC	P		V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 0	2.0	—	7.4	
	CC	C		V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 1	2.7	—	9.7	
	CC	C		V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 1	2.5	—	9.2	
V_{FXOSC}	CC	T	Oscillation amplitude at EXTAL	f_{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0	1.3	—	—	V
				f_{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1	1.3	—	—	
$V_{FXOSCOP}$	CC	C	Oscillation operating point	—	—	0.95	—	V
I_{FXOSC}[2]	CC	T	Fast external crystal oscillator consumption	—	—	2	3	mA

Table 37. Fast external crystal oscillator (4 to 20 MHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
$t_{FXOSCSU}$	CC	T	Fast external crystal oscillator start-up time	f_{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0	—	—	6	ms
				f_{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1	—	—	1.8	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	Oscillator bypass mode	$0.65V_{DD}$	—	V_{DD} + 0.4	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	Oscillator bypass mode	−0.4	—	$0.35V_{DD}$	V

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified.

2 Stated values take into account only analog module consumption but not the digital contributor (clock tree and enabled peripherals).

3 High gain is required to config in software for the 20 MHz crystal external oscillator

4.12 Slow external crystal oscillator (32 kHz) electrical characteristics

The device provides a low power oscillator/resonator driver.

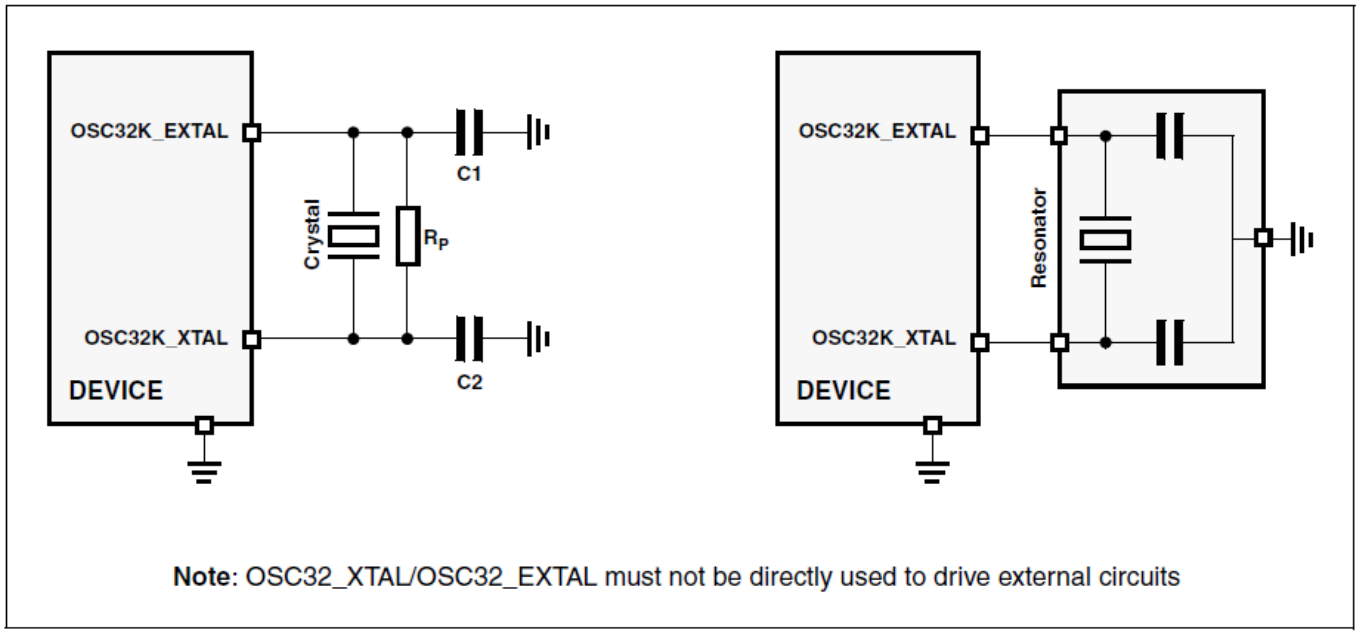


Figure 14. Crystal oscillator and resonator connection scheme

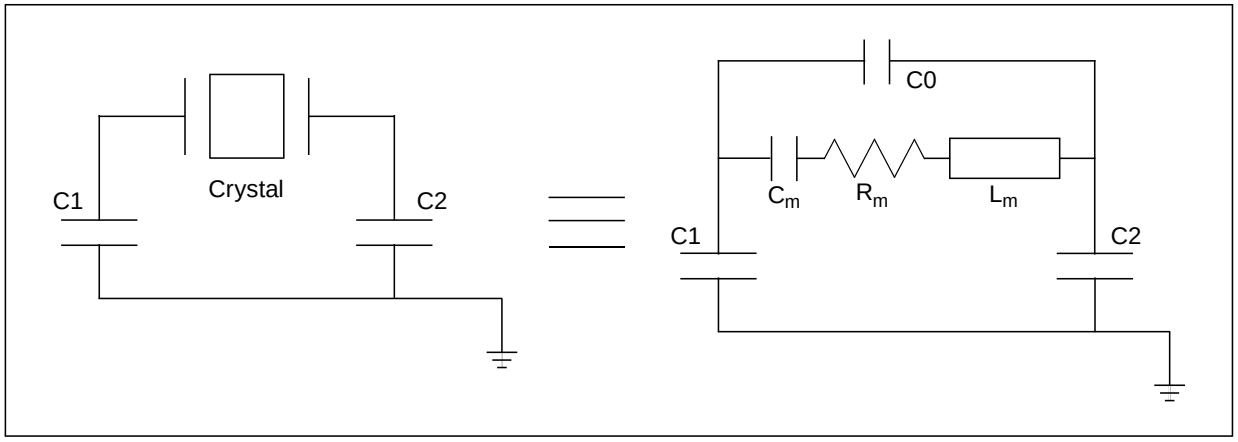


Figure 15. Equivalent circuit of a quartz crystal

Table 38. Crystal motional characteristics[1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
L_m	Motional inductance	—	—	11.796	—	KH
C_m	Motional capacitance	—	—	2	—	fF
C1/C2	Load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground[2]	—	18	—	28	pF
R_m [3]	Motional resistance	AC coupled at C0 = 2.85 pF [4]	—	—	65	kΩ
		AC coupled at C0 = 4.9 pF[4]	—	—	50	
		AC coupled at C0 = 7.0 pF[4]	—	—	35	
		AC coupled at C0 = 9.0 pF[4]	—	—	30	

1 The crystal used is Epson Toyocom MC306.

2 This is the recommended range of load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground. It includes all the parasitics due to board traces, crystal and package.

3 Maximum ESR (R_m) of the crystal is 50 kΩ

4 C0 Includes a parasitic capacitance of 2.0 pF between OSC32K_XTAL and OSC32K_EXTAL pins.

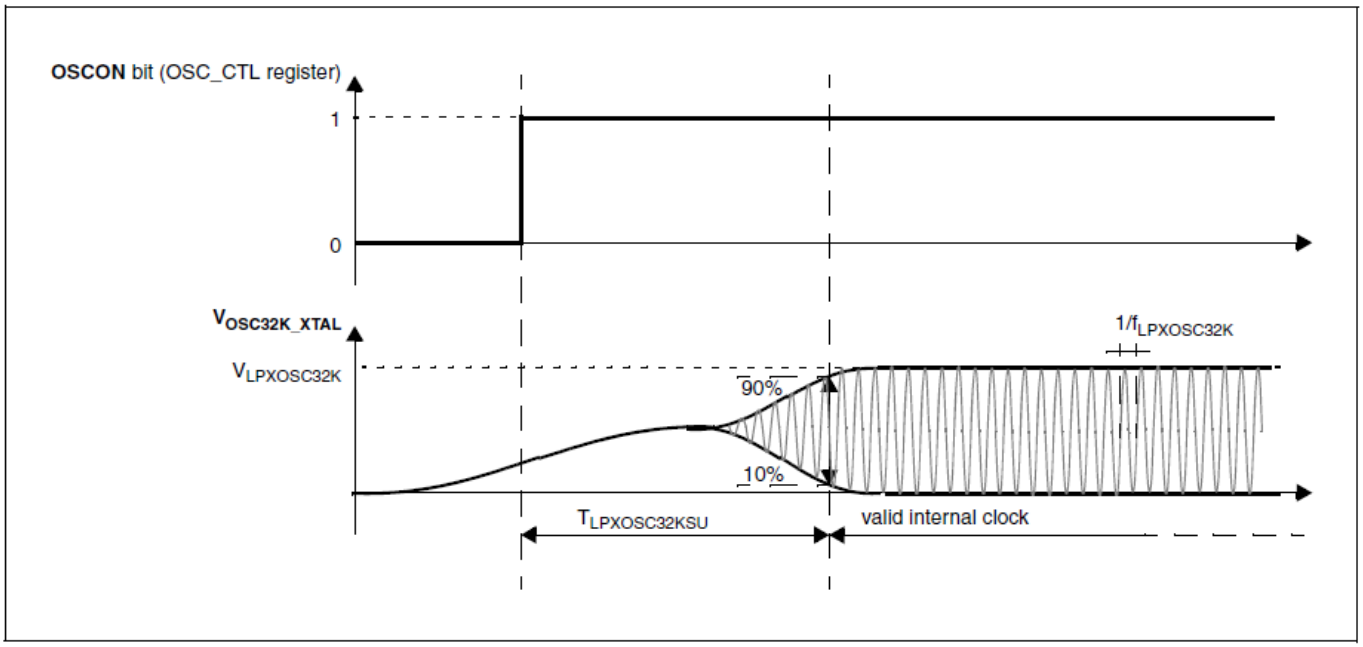


Figure 16. Slow external crystal oscillator (32 kHz) timing diagram

Table 39. Slow external crystal oscillator (32 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{SXOSC}	SR	—	Slow external crystal oscillator frequency	—	32	32.768	40	kHz
V_{SXOSC}	CC	T	Oscillation amplitude	—	—	2.1	—	V
$I_{SXOSCBIAS}$	CC	T	Oscillation bias current	—		2.5		µA
I_{SXOSC}	CC	T	Slow external crystal oscillator consumption	—	—	—	8	µA
$t_{SXOSCSU}$	CC	T	Slow external crystal oscillator start-up time	—	—	—	2[2]	s

[1] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified. Values are specified for no neighbor GPIO pin activity. If oscillator is enabled (OSC32K_XTAL and OSC32K_EXTAL pins), neighboring pins should not toggle.

[2] Start-up time has been measured with EPSON TOYOCOM MC306 crystal. Variation may be seen with other crystal.

4.13 FMPLL electrical characteristics

The device provides a frequency modulated phase locked loop (FMPLL) module to generate a fast system clock from the main oscillator driver.

Table 40. FMPLL electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	FMPLL reference clock[2]	—	4	—	64	MHz
Δ_{PLLIN}	SR	—	FMPLL reference clock duty cycle[2]	—	40	—	60	%
f_{PLLOUT}	CC	P	FMPLL output clock frequency	—	16	—	64	MHz
f_{VCO}[3]	CC	P	VCO frequency without frequency modulation	—	256	—	512	MHz
		P	VCO frequency with frequency modulation	—	245.76	—	532.48	
f_{CPU}	SR	—	System clock frequency	—	—	—	64	MHz
f_{FREE}	CC	P	Free-running frequency	—	20	—	150	MHz
t_{LOCK}	CC	P	FMPLL lock time	Stable oscillator (f_{PLLIN} = 16 MHz)		40	150	µs
Δt_{STJIT}	CC	—	FMPLL short term jitter[4]	f_{sys} maximum	–4	—	4	%
Δt_{LTJIT}	CC	—	FMPLL long term jitter	f_{PLLCLK} at 64 MHz, 4000 cycles	—	—	10	ns
I_{PLL}	CC	C	FMPLL consumption	T_A = 25 °C	—	—	4	mA

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified

2 PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.

3 Frequency modulation is considered ± 4%.

4 Short term jitter is measured on the clock rising edge at cycle n and n+4.

4.14 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz main internal RC oscillator. This is used as the default clock at the power-up of the device.

Table 41. Fast internal RC oscillator (16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{FIRC}	CC	P	Fast internal RC oscillator high frequency	T_A = 25 °C, trimmed	—	16	—	MHz
	SR	—		—	12		20	
$I_{FIRCRUN}$[2],	CC	T	Fast internal RC oscillator high frequency current in running mode	T_A = 25 °C, trimmed	—	—	200	µA
$I_{FIRCPWD}$	CC	D	Fast internal RC oscillator high frequency current in power down mode	T_A = 25 °C	—	—	10	µA

Table 41. Fast internal RC oscillator (16 MHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
$I_{FIRCSTOP}$	CC	T	Fast internal RC oscillator high frequency and system clock current in stop mode	T_A = 25 °C	sysclk = off	—	500	—	µA
					sysclk = 2 MHz	—	600	—	
					sysclk = 4 MHz	—	700	—	
					sysclk = 8 MHz	—	900	—	
					sysclk = 16 MHz	—	1250	—	
t_{FIRCSU}	CC	C	Fast internal RC oscillator start-up time	V_{DD} = 5.0 V ± 10%		—	1.1	2.0	µs
$\Delta_{FIRCPRE}$	CC	C	Fast internal RC oscillator precision after software trimming of f_{FIRC}	T_A = 25 °C		−1	—	1	%
$\Delta_{FIRCTRIM}$	CC	C	Fast internal RC oscillator trimming step	T_A = 25 °C		—	1.6		%
$\Delta_{FIRCVAR}$	CC	C	Fast internal RC oscillator variation over temperature and supply with respect to f_{FIRC} at T_A = 25 °C in high-frequency configuration	—		−5	—	5	%

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified

2 This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

4.15 Slow internal RC oscillator (128 kHz) electrical characteristics

The device provides a 128 kHz low power internal RC oscillator. This can be used as the reference clock for the RTC module.

Table 42. Slow internal RC oscillator (128 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{SIRC}	CC	P	Slow internal RC oscillator low frequency	T_A = 25 °C, trimmed	—	128	—	kHz
	SR	—		—	100	—	150	
I_{SIRC}[2],	CC	C	Slow internal RC oscillator low frequency current	T_A = 25 °C, trimmed	—	—	5	µA
t_{SIRCSU}	CC	P	Slow internal RC oscillator start-up time	T_A = 25 °C, V_{DD} = 5.0 V ± 10%	—	8	12	µs
$\Delta_{SIRCPRE}$	CC	C	Slow internal RC oscillator precision after software trimming of f_{SIRC}	T_A = 25 °C	−2	—	2	%
$\Delta_{SIRCTRIM}$	CC	C	Slow internal RC oscillator trimming step	—	—	2.7	—	

Table 42. Slow internal RC oscillator (128 kHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
$\Delta_{SIRCVAR}$	CC	C	Slow internal RC oscillator variation in temperature and supply with respect to f_{SIRC} at T_A = 55 °C in high frequency configuration	High frequency configuration	−10	—	10	%

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified

2 This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

4.16 ADC electrical characteristics

4.16.1 Introduction

The device provides two Successive Approximation Register (SAR) analog-to-digital converters (10-bit).

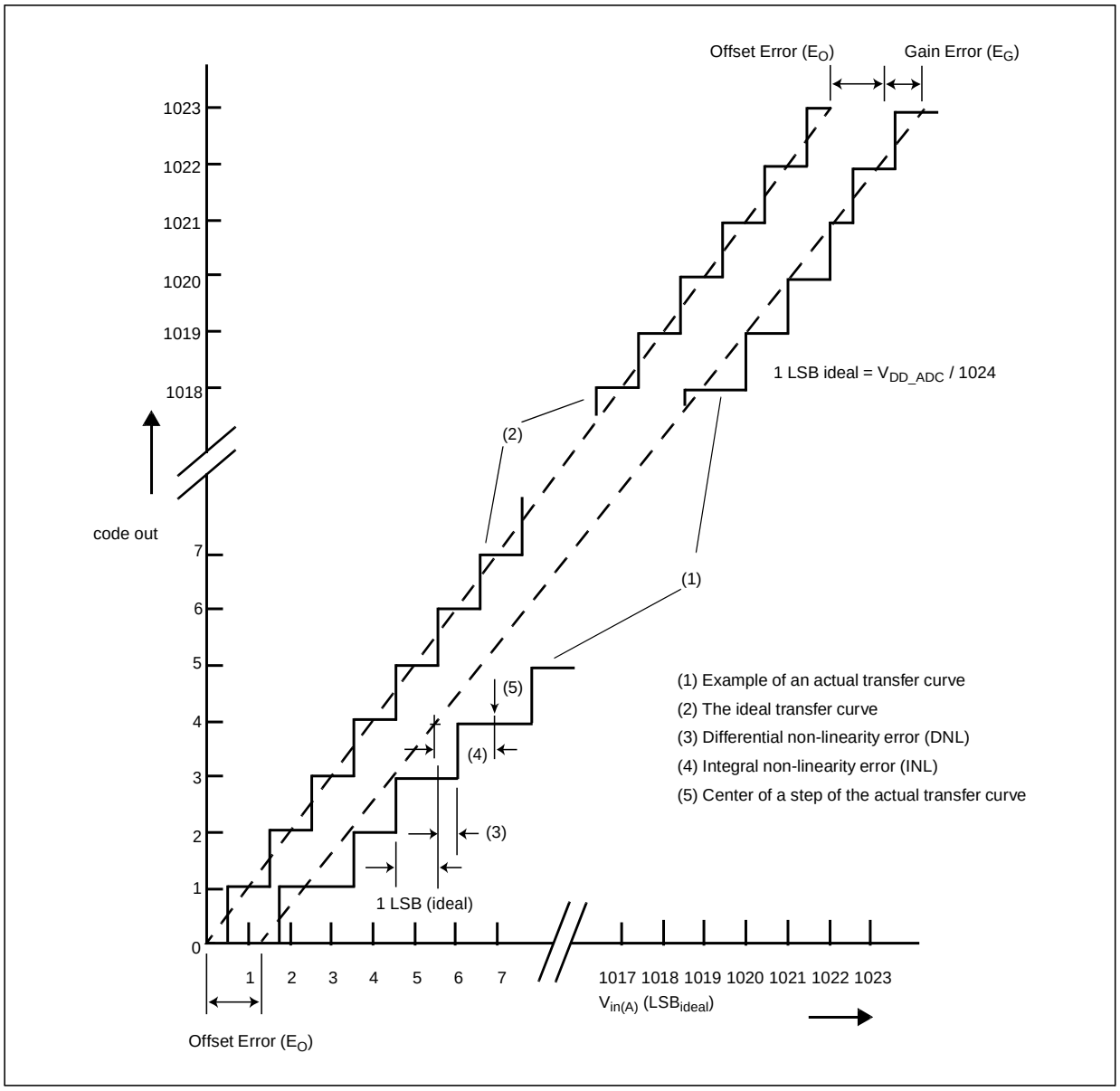


Figure 17. ADC_0 characteristic and error definitions

4.16.2 Input impedance and ADC accuracy

In the following analysis, the input circuit corresponding to the precise channels is considered.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer

or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: being C_S and C_{p2} substantially two switched capacitances, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S+C_{p2} equal to 3 pF, a resistance of 330 kΩ is obtained (R_{EQ} = 1 / (f_c × (C_S+C_{p2})), where f_c represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S+C_{p2}) and the sum of R_S + R_F, the external circuit must be designed to respect the Equation 4:

$$V_A \bullet \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2}\text{LSB} \qquad \textit{Eqn. 4}$$

Equation 4 generates a constraint for external network design, in particular on a resistive path.

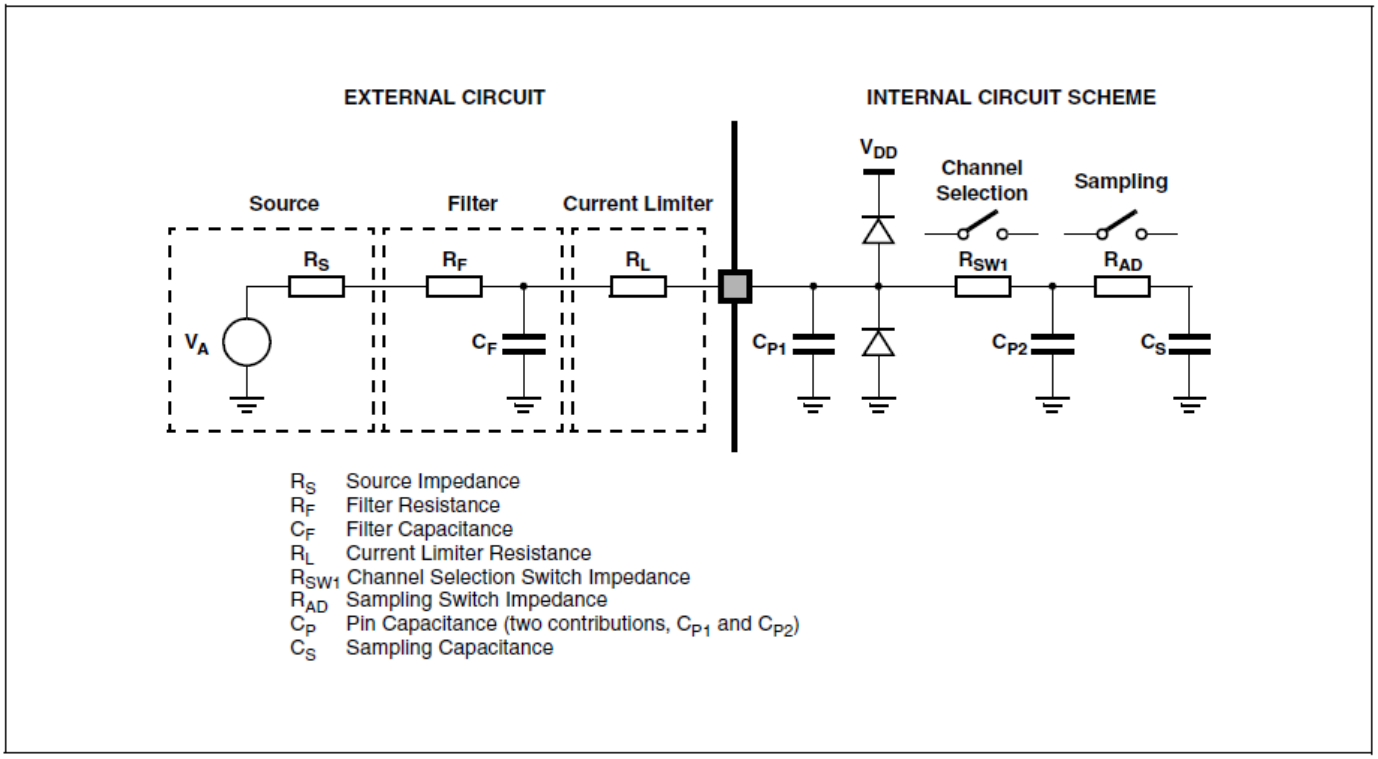


Figure 18. Input equivalent circuit (precise channels)

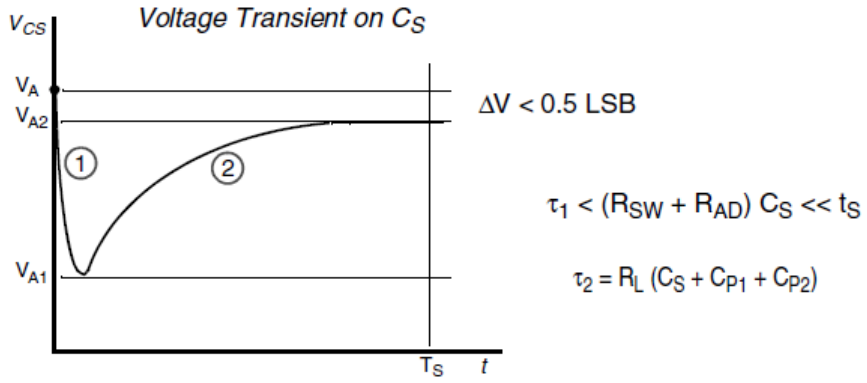


Figure 19. **Input equivalent circuit (extended channels)**

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 18): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

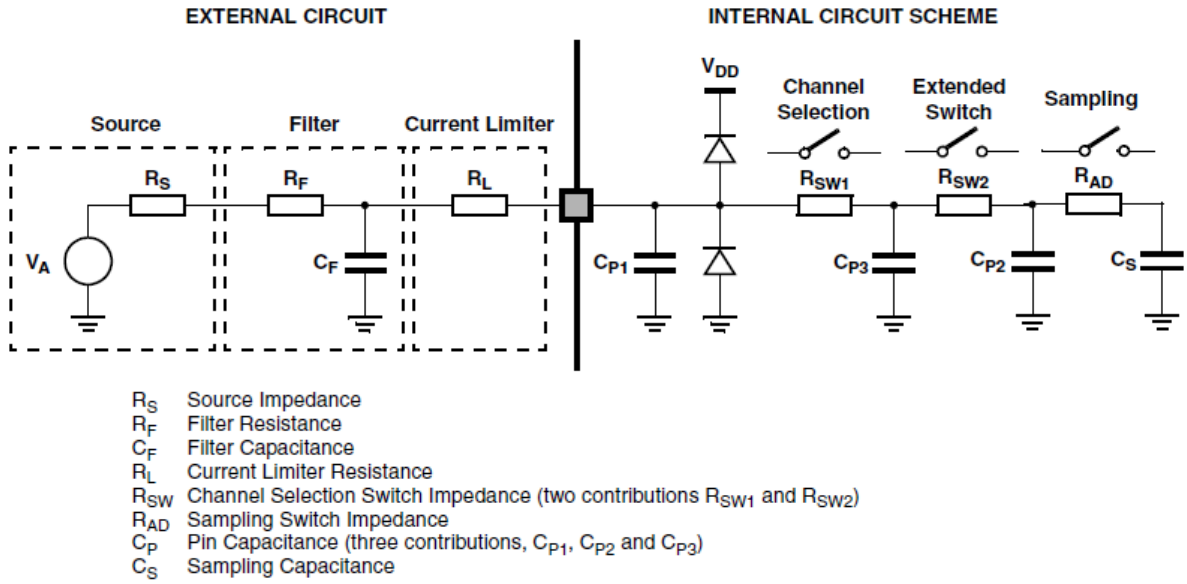


Figure 20. **Transient behavior during sampling phase**

In particular two different transient periods can be distinguished:

1. A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S} \qquad \textit{Eqn. 5}$$

   Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time t_S is always much longer than the internal time constant:

Eqn. 6

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll t_s$$

   The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to Equation 7:

Eqn. 7

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

2. A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Eqn. 8

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time t_s, a constraints on R_L sizing is obtained:

ADC_0 (10-bit) ***Eqn. 9***

$$8.5 \bullet \tau_2 = 8.5 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < t_s$$

ADC_1 (12-bit) ***Eqn. 10***

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < t_s$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. Equation 11 must be respected (charge balance assuming now C_S already charged at V_{A1}):

Eqn. 11

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the R_FC_F filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant R_FC_F of the filter is very high with respect to the sampling time (t_s). The filter is typically designed to act as antialiasing.

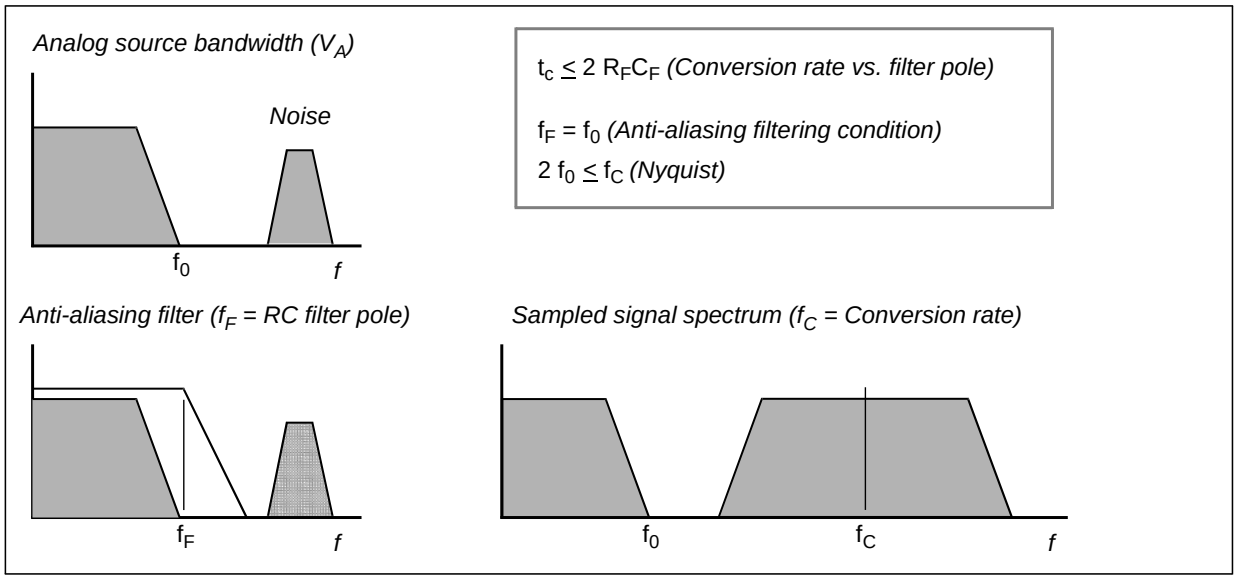


Figure 21. Spectral representation of input signal

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the antialiasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (t_c). Again the conversion period t_c is longer than the sampling time t_s, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter R_FC_F is definitively much higher than the sampling time t_s, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive Equation 12 between the ideal and real sampled voltage on C_S:

Eqn. 12

$$\frac{V_{A2}}{V_A} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

ADC_0 (10-bit) ***Eqn. 13***

$$C_F > 2048 \bullet C_S$$

ADC_1 (12-bit) ***Eqn. 14***

$$C_F > 8192 \bullet C_S$$

4.16.3 ADC electrical characteristics

Table 43. ADC input leakage current

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
I_{LKG}	CC	D	Input leakage current	T_A = −40 °C	No current injection on adjacent pin	—	1	70	nA
		D		T_A = 25 °C		—	1	70	
		D		T_A = 85 °C			3	100	
		D		T_A = 105 °C		—	8	200	
		P		T_A = 125 °C		—	45	400	

Table 44. ADC_0 conversion characteristics (10-bit ADC_0)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{SS_ADC0}	SR	—	Voltage on VSS_HV_ADC0 (ADC_0 reference) pin with respect to ground (V_{SS})[2]	—	−0.1	—	0.1	V
V_{DD_ADC0}	SR	—	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	V_{DD} − 0.1	—	V_{DD} + 0.1	V
V_{AINx}	SR	—	Analog input voltage[3]	—	V_{SS_ADC0} − 0.1	—	V_{DD_ADC0} + 0.1	V
$I_{ADC0pwd}$	SR	—	ADC_0 consumption in power down mode	—	—	—	50	µA
$I_{ADC0run}$	SR	—	ADC_0 consumption in running mode	—	—	—	5	mA
f_{ADC0}	SR	—	ADC_0 analog frequency	—	6	—	32 + 4%	MHz
Δ_{ADC0_SYS}	SR	—	ADC_0 digital clock duty cycle (ipg_clk)	ADCLKSEL = 1[4]	45	—	55	%
t_{ADC0_PU}	SR	—	ADC_0 power up delay	—	—	—	1.5	µs
t_{ADC0_S}	CC	T	Sampling time[5]	f_{ADC} = 32 MHz, INPSAMP = 17	0.5	—		µs
				f_{ADC} = 6 MHz, INPSAMP = 255	—	—	42	

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
t_{ADC0_C}	CC	P	Conversion time[6]	f_{ADC} = 32 MHz, INPCMP = 2		0.625	—	—	µs
C_S	CC	D	ADC_0 input sampling capacitance	—		—	—	3	pF
C_{P1}	CC	D	ADC_0 input pin capacitance 1	—		—	—	3	pF
C_{P2}	CC	D	ADC_0 input pin capacitance 2	—		—	—	1	pF
C_{P3}	CC	D	ADC_0 input pin capacitance 3	—		—	—	1	pF
R_{SW1}	CC	D	Internal resistance of analog source	—		—	—	3	kΩ
R_{SW2}	CC	D	Internal resistance of analog source	—		—	—	2	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—		—	—	2	kΩ
I_{INJ}	SR	—	Input current Injection	Current injection on one ADC_0 input, different from the converted one	V_{DD} = 3.3 V ± 10%	−5	—	5	mA
					V_{DD} = 5.0 V ± 10%	−5	—	5	
| INL |	CC	T	Absolute integral nonlinearity	No overload		—	0.5	1.5	LSB
| DNL |	CC	T	Absolute differential nonlinearity	No overload		—	0.5	1.0	LSB
$\| E_O \|$	CC	T	Absolute offset error	—		—	0.5	—	LSB
$\| E_G \|$	CC	T	Absolute gain error	—		—	0.6	—	LSB
TUEP	CC	P	Total unadjusted error[7] for precise channels, input only pins	Without current injection		−2	0.6	2	LSB
		T		With current injection		−3	—	3	
TUEX	CC	T	Total unadjusted error[7] for extended channel	Without current injection		−3	1	3	LSB
		T		With current injection		−4		4	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified.

2 Analog and digital V_{SS} **must** be common (to be tied together externally).

3 V_{AINx} may exceed V_{SS_ADC0} and V_{DD_ADC0} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.

4 Duty cycle is ensured by using system clock without prescaling. When ADCLKSEL = 0, the duty cycle is ensured by internal divider by 2.

5 During the sampling time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC0_S}. After the end of the sampling time t_{ADC0_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sampling clock t_{ADC0_S} depend on programming.

6 This parameter does not include the sampling time t_{ADC0_S}, but only the time for determining the digital result and the time to load the result's register with the conversion result.

7 Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

Table 44. ADC_0 conversion characteristics (10-bit ADC_0) (continued)

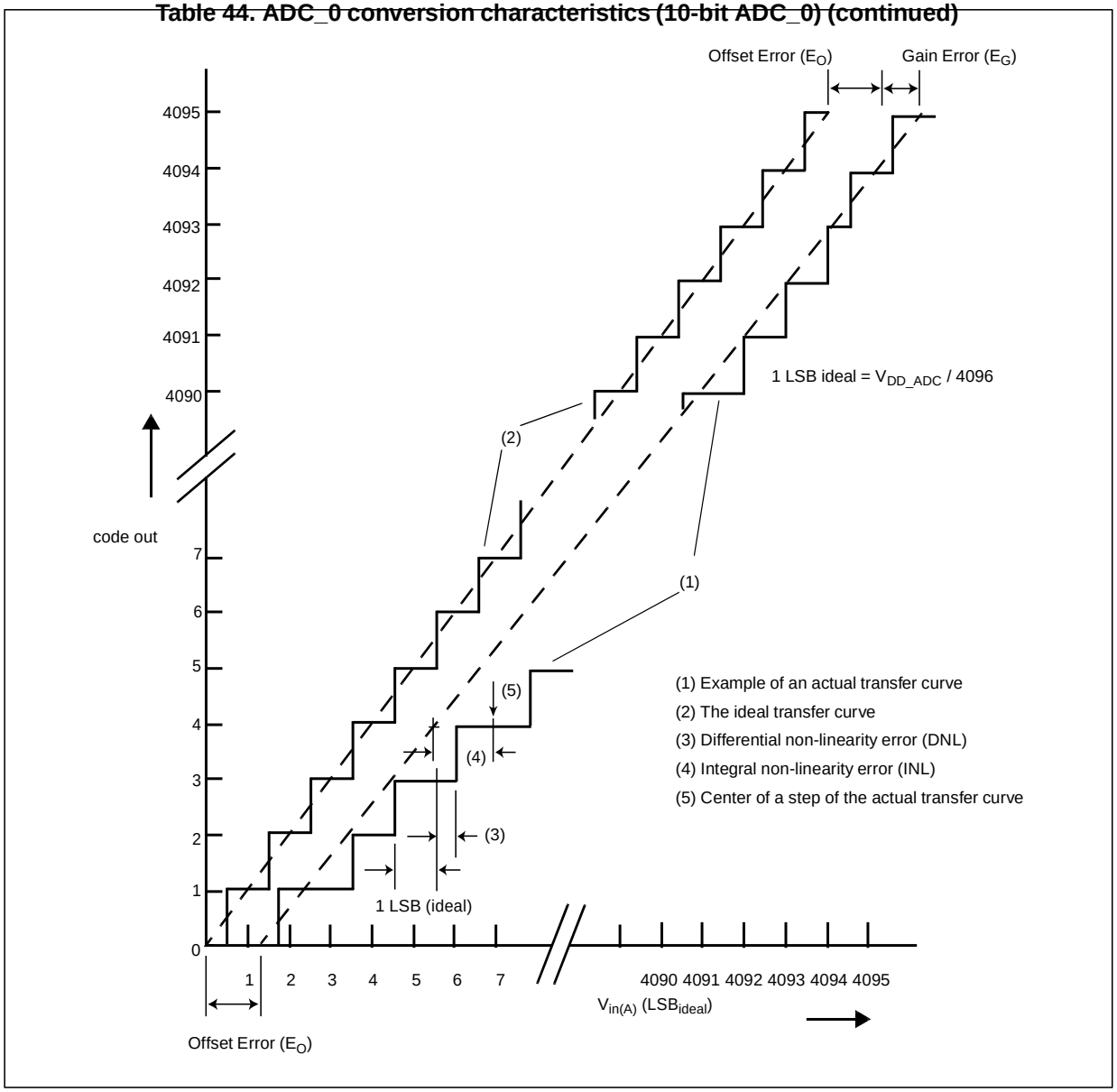


Figure 22. ADC_1 characteristic and error definitions

Table 45. ADC_1 conversion characteristics (12-bit ADC_1)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{SS_ADC1}	SR	—	Voltage on VSS_HV_ADC1 (ADC_1 reference) pin with respect to ground (V_{SS})[2]	—	–0.1	—	0.1	V
V_{DD_ADC1}	SR	—	Voltage on VDD_HV_ADC1 pin (ADC_1 reference) with respect to ground (V_{SS})	—	V_{DD} – 0.1	—	V_{DD} + 0.1	V

Table 45. ADC_1 conversion characteristics (12-bit ADC_1) (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{AINx}	SR	—	Analog input voltage[3]	—	V_{SS_ADC1} – 0.1	—	V_{DD_ADC1} + 0.1	V
$I_{ADC1pwd}$	SR	—	ADC_1 consumption in power down mode	—	—	—	50	µA
$I_{ADC1run}$	SR	—	ADC_1 consumption in running mode	—	—	—	6	mA
f_{ADC1}	SR	—	ADC_1 analog frequency	V_{DD} = 3.3 V	3.33	—	20 + 4%	MHz
				V_{DD} = 5 V	3.33	—	32 + 4%	
t_{ADC1_PU}	SR	—	ADC_1 power up delay	—	—	—	1.5	µs
t_{ADC1_S}	CC	T	Sampling time[4] V_{DD} = 3.3 V	f_{ADC1} = 20 MHz, INPSAMP = 12	600	—	—	ns
			Sampling time[4] V_{DD} = 5.0 V	f_{ADC1} = 32 MHz, INPSAMP = 17	500	—	—	
			Sampling time[4] V_{DD} = 3.3 V	f_{ADC1} = 3.33 MHz, INPSAMP = 255	—	—	76.2	µs
			Sampling time[4] V_{DD} = 5.0 V	f_{ADC1} = 3.33 MHz, INPSAMP = 255	—	—	76.2	
t_{ADC1_C}	CC	P	Conversion time[5] V_{DD} = 3.3 V	f_{ADC1} = 20 MHz, INPCMP = 0	2.4	—	—	µs
			Conversion time[5] V_{DD} = 5.0 V	$f_{ADC\ 1}$ = 32 MHz, INPCMP = 0	1.5	—	—	µs
			Conversion time[5] V_{DD} = 3.3 V	$f_{ADC\ 1}$ = 13.33 MHz, INPCMP = 0	—	—	3.6	µs
			Conversion time[5] V_{DD} = 5.0 V	f_{ADC1} = 13.33 MHz, INPCMP = 0	—	—	3.6	µs
Δ_{ADC1_SYS}	SR	—	ADC_1 digital clock duty cycle	ADCLKSEL = 1[6]	45	—	55	%
C_S	CC	D	ADC_1 input sampling capacitance	—	—	—	5	pF
C_{P1}	CC	D	ADC_1 input pin capacitance 1	—	—	—	3	pF
C_{P2}	CC	D	ADC_1 input pin capacitance 2	—	—	—	1	pF
C_{P3}	CC	D	ADC_1 input pin capacitance 3	—	—	—	1.5	pF
R_{SW1}	CC	D	Internal resistance of analog source	—	—	—	1	kΩ
R_{SW2}	CC	D	Internal resistance of analog source	—	—	—	2	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—	—	—	0.3	kΩ

Table 45. ADC_1 conversion characteristics (12-bit ADC_1) (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{INJ}	SR	—	Input current Injection	Current injection on one ADC_1 input, different from the converted one	V_{DD} = 3.3 V ± 10%	–5	—	5	mA
					V_{DD} = 5.0 V ± 10%	–5	—	5	
| INLP |	CC	T	Absolute integral nonlinearity – Precise channels	No overload		—	1	3	LSB
| INLX |	CC	T	Absolute integral nonlinearity – Extended channels	No overload		—	1.5	5	LSB
| DNL |	CC	T	Absolute differential nonlinearity	No overload		—	0.5	1	LSB
$\| E_O \|$	CC	T	Absolute offset error	—		—	2	—	LSB
$\| E_G \|$	CC	T	Absolute gain error	—		—	2	—	LSB
TUEP[7]	CC	P	Total unadjusted error for precise channels, input only pins	Without current injection		–6	—	6	LSB
		T		With current injection		–8	—	8	
TUEX[7]	CC	T	Total unadjusted error for extended channel	Without current injection		–10	—	10	LSB
		T		With current injection		–12	—	12	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 Analog and digital V_{SS} **must** be common (to be tied together externally).

3 V_{AINx} may exceed V_{SS_ADC1} and V_{DD_ADC1} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0xFFF.

4 During the sampling time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC1_S}. After the end of the sampling time t_{ADC1_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sampling clock t_{ADC1_S} depend on programming.

5 This parameter does not include the sampling time t_{ADC1_S}, but only the time for determining the digital result and the time to load the result's register with the conversion result.

6 Duty cycle is ensured by using system clock without prescaling. When ADCLKSEL = 0, the duty cycle is ensured by internal divider by 2.

7 Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

4.17 On-chip peripherals

4.17.1 Current consumption

Table 46. On-chip peripherals current consumption[1]

Symbol		C	Parameter	Conditions		Typical value[2]	Unit
$I_{DD\_BV(CAN)}$	CC	T	CAN (FlexCAN) supply current on V_{DD_BV}	Bitrate: 500 Kbyte/s	Total (static + dynamic) consumption: • FlexCAN in loop-back mode • XTAL at 8 MHz used as CAN engine clock source • Message sending period is 580 µs	8 * f_{periph} + 85	µA
				Bitrate: 125 Kbyte/s		8 * f_{periph} + 27	
$I_{DD\_BV(eMIOS)}$	CC	T	eMIOS supply current on V_{DD_BV}	Static consumption: • eMIOS channel OFF • Global prescaler enabled		29 * f_{periph}	µA
				Dynamic consumption: • It does not change varying the frequency (0.003 mA)		3	
$I_{DD\_BV(SCI)}$	CC	T	SCI (LINFlex) supply current on V_{DD_BV}	Total (static + dynamic) consumption: • LIN mode • Baudrate: 20 Kbyte/s		5 * f_{periph} + 31	µA
$I_{DD\_BV(SPI)}$	CC	T	SPI (DSPI) supply current on V_{DD_BV}	Ballast static consumption (only clocked)		1	µA
				Ballast dynamic consumption (continuous communication): • Baudrate: 2 Mbit/s • Transmission every 8 µs • Frame: 16 bits		16 * f_{periph}	
I_{DD_BV} (ADC_0/ADC_1)	CC	T	ADC_0/ADC_1 supply current on V_{DD_BV}	V_{DD} = 5.5 V	Ballast static consumption (no conversion)[3]	41 * f_{periph}	µA
					Ballast dynamic consumption (continuous conversion)[3]	46 * f_{periph}	
$I_{DD\_HV\_ADC0}$	CC	T	ADC_0 supply current on $V_{DD\_HV\_ADC0}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	200	µA
					Analog dynamic consumption (continuous conversion)	3	mA
$I_{DD\_HV\_ADC1}$	CC	T	ADC_1 supply current on $V_{DD\_HV\_ADC1}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	300 * f_{periph}	µA
					Analog dynamic consumption (continuous conversion)	4	mA
$I_{DD\_HV(FLASH)}$	CC	T	CFlash + DFlash supply current on V_{DD_HV}	V_{DD} = 5.5 V	—	12	mA
$I_{DD\_HV(PLL)}$	CC	T	PLL supply current on V_{DD_HV}	V_{DD} = 5.5 V	—	30 * f_{periph}	µA

1 Operating conditions: T_A = 25 °C, fperiph = 8 MHz to 64 MHz

2 fperiph is an absolute value.

3 During the conversion, the total current consumption is given from the sum of the static and dynamic consumption i.e. (41 + 46) * fperiph'

4.17.2 DSPI characteristics

Table 47. DSPI characteristics[1]

No.	Symbol		C	Parameter		DSPI0/DSPI1			Unit
						Min	Typ	Max	
1	t_{SCK}	SR	D	SCK cycle time	Master mode (MTFE = 0)	125	—	—	ns
			D		Slave mode (MTFE = 0)	125	—	—	
			D		Master mode (MTFE = 1)	83	—	—	
			D		Slave mode (MTFE = 1)	83	—	—	
—	f_{DSPI}	SR	D	DSPI digital controller frequency		—	—	f_{CPU}	MHz
—	Δt_{CSC}	CC	D	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->0	Master mode	—	—	130[2]	ns
—	Δt_{ASC}	CC	D	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->1	Master mode	—	—	130[3]	ns
2	$t_{CSCe_{xt}}$[4]	SR	D	CS to SCK delay	Slave mode	32	—	—	ns
3	t_{ASCext}[5]	SR	D	After SCK delay	Slave mode	$1/f_{DSPI} + 5$	—	—	ns_{DSPI}
4	t_{SDC}	CC	D	SCK duty cycle	Master mode	—	$t_{SCK}/2$	—	ns
		SR	D		Slave mode	$t_{SCK}/2$	—	—	
5	t_A	SR	D	Slave access time	Slave mode	—	—	$1/f_{DSPI} + 70$	ns
6	t_{DI}	SR	D	Slave SOUT disable time	Slave mode	7	—	—	ns
7	t_{PCSC}	SR	D	PCSx to $\overline{PCSS}$ time	—	0	—	—	ns
8	t_{PASC}	SR	D	PCSS to PCSx time	—	0	—	—	ns
9	t_{SUI}	SR	D	Data setup time for inputs	Master mode	43	—	—	ns
					Slave mode	5	—	—	

Table 47. DSPI characteristics[1] (continued)

No.	Symbol		C	Parameter		DSPI0/DSPI1			Unit
						Min	Typ	Max	
10	t_{HI}	SR	D	Data hold time for inputs	Master mode	0	—	—	ns
					Slave mode	2[6]	—	—	
11	t_{SUO}[7]	CC	D	Data valid after SCK edge	Master mode	—	—	32	ns
					Slave mode	—	—	52	
12	t_{HO}[7]	CC	D	Data hold time for outputs	Master mode	0	—	—	ns
					Slave mode	8	—	—	

1 Operating conditions: C_L = 10 to 50 pF, $Slew_{IN}$ = 3.5 to 15 ns

2 Maximum value is reached when CSn pad is configured as SLOW pad while SCK pad is configured as MEDIUM. A positive value means that SCK starts before CSn is asserted. DSPI2 has only SLOW SCK available.

3 Maximum value is reached when CSn pad is configured as MEDIUM pad while SCK pad is configured as SLOW. A positive value means that CSn is deasserted before SCK. DSPI0 and DSPI1 have only MEDIUM SCK available.

4 The t_{CSC} delay value is configurable through a register. When configuring t_{CSC} (using PCSSCK and CSSCK fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{CSC} to ensure positive t_{CSCext}.

5 The t_{ASC} delay value is configurable through a register. When configuring t_{ASC} (using PASC and ASC fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{ASC} to ensure positive t_{ASCext}.

6 This delay value corresponds to SMPL_PT = 00b which is bit field 9 and 8 of DSPI_MCR register.

7 SCK and SOUT are configured as MEDIUM pad.

Figure 22. DSPI classic SPI timing — master, CPHA = 0

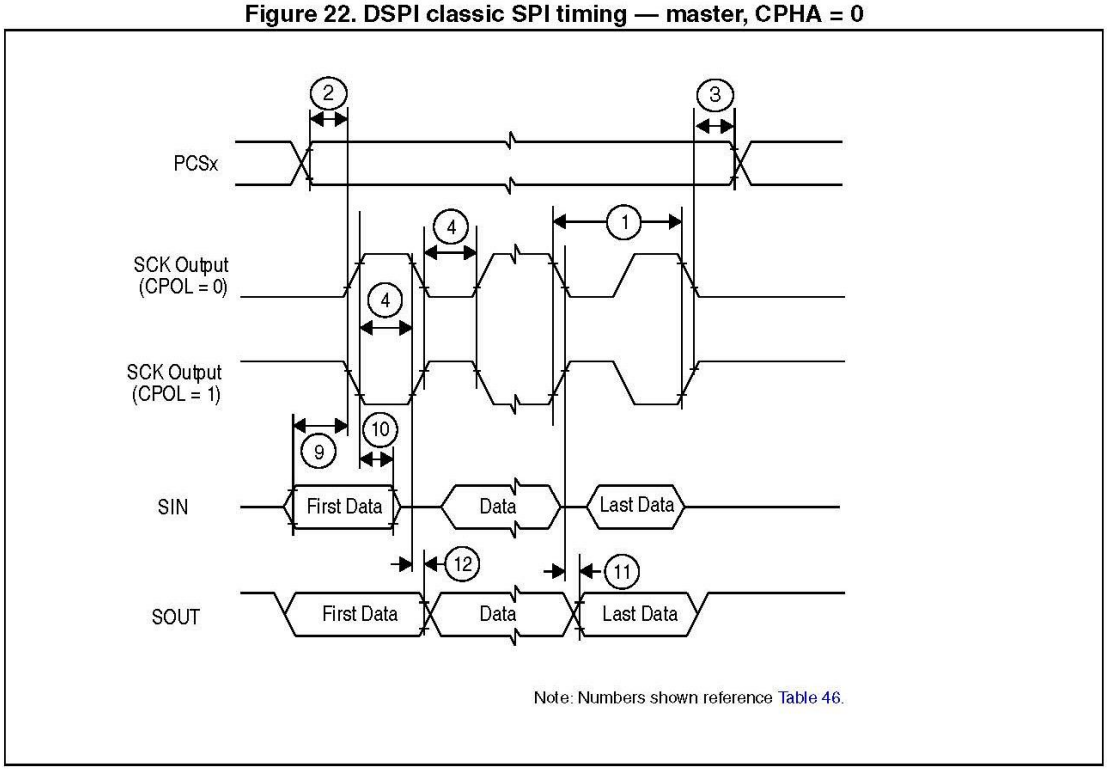


Figure 23. DSPI classic SPI timing — master, CPHA = 1

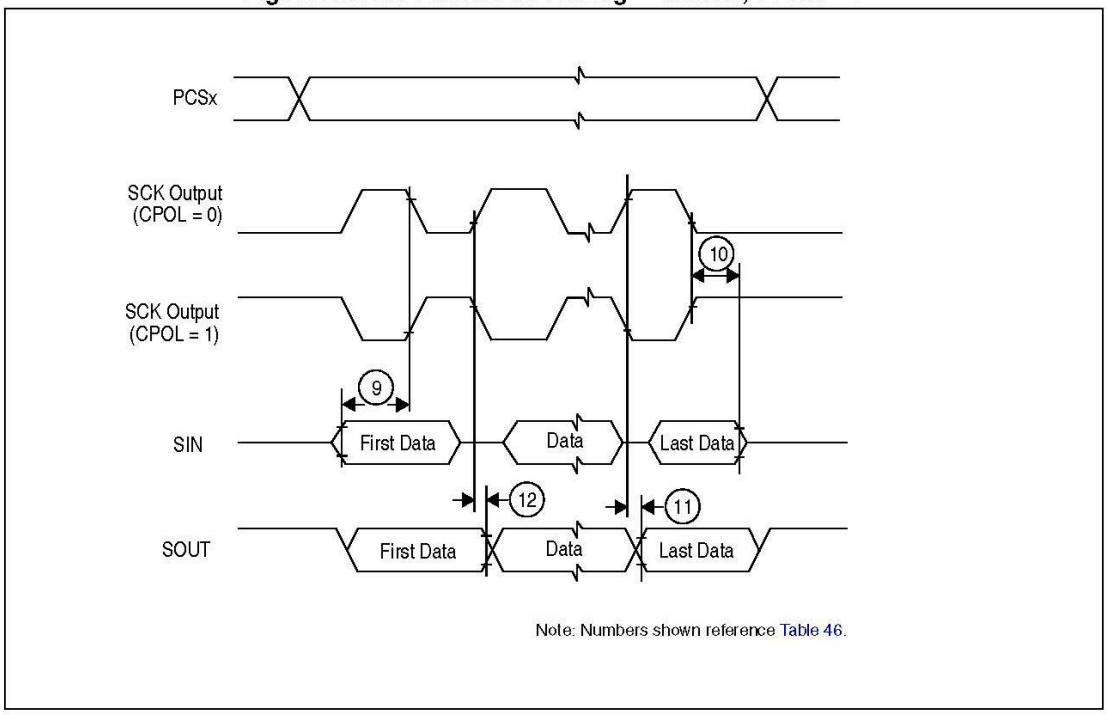


Figure 24. DSPI classic SPI timing — slave, CPHA = 0

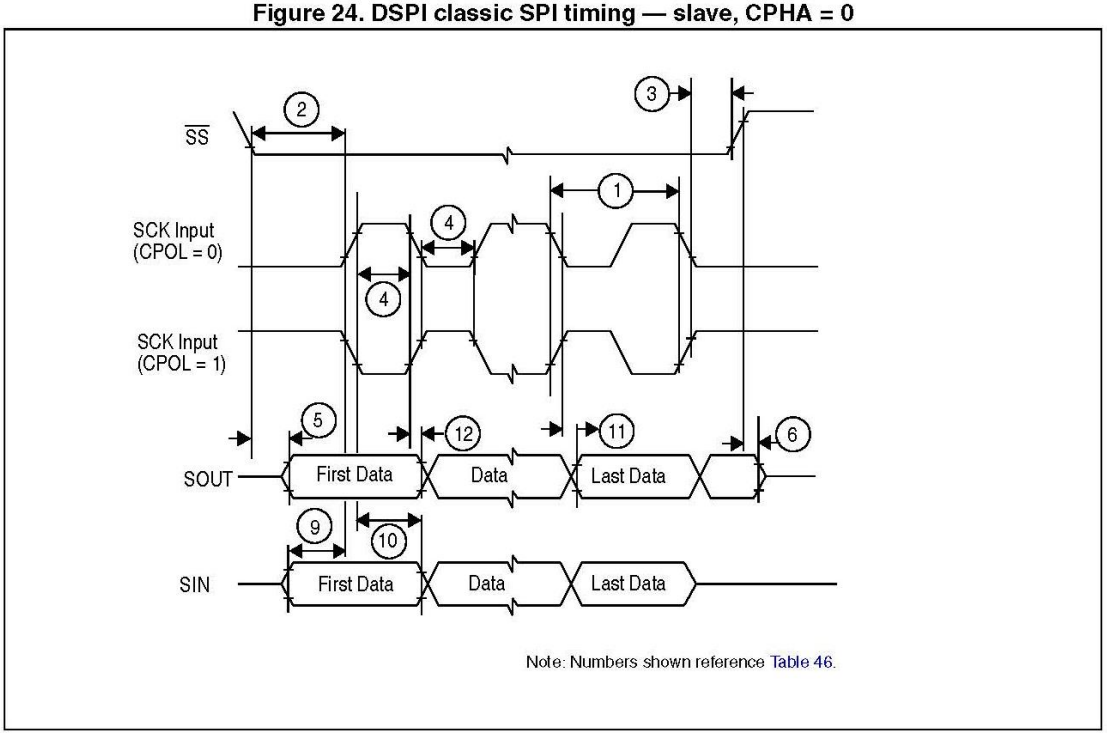


Figure 25. DSPI classic SPI timing — slave, CPHA = 1

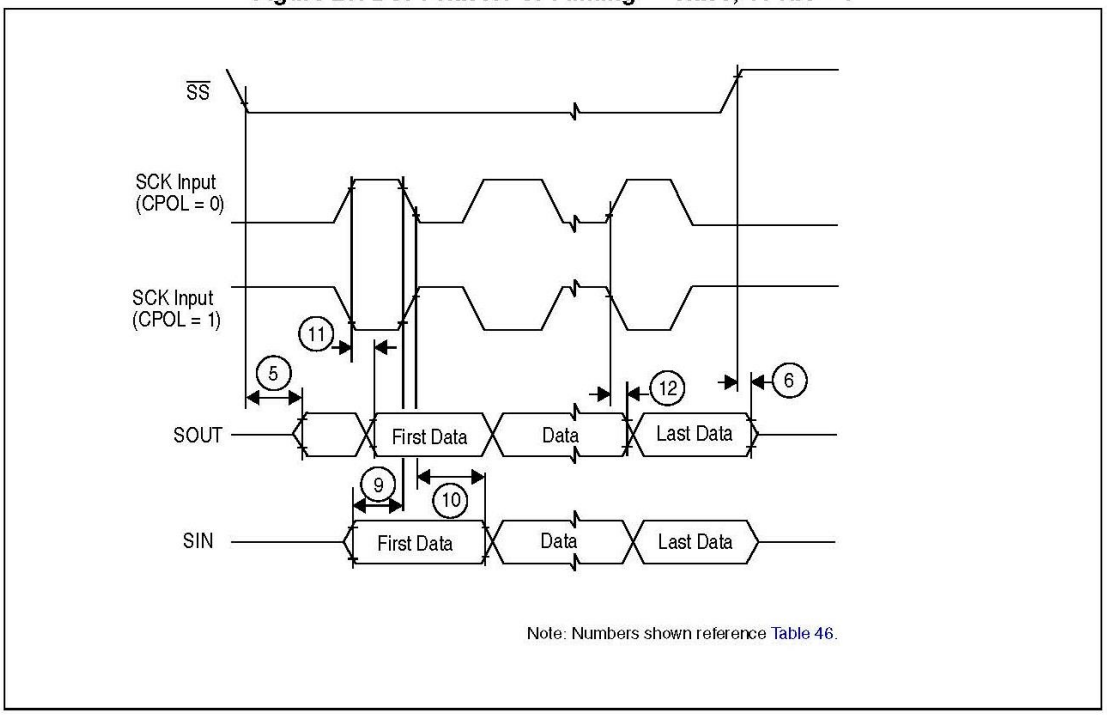


Figure 26. DSPI modified transfer format timing — master, CPHA = 0

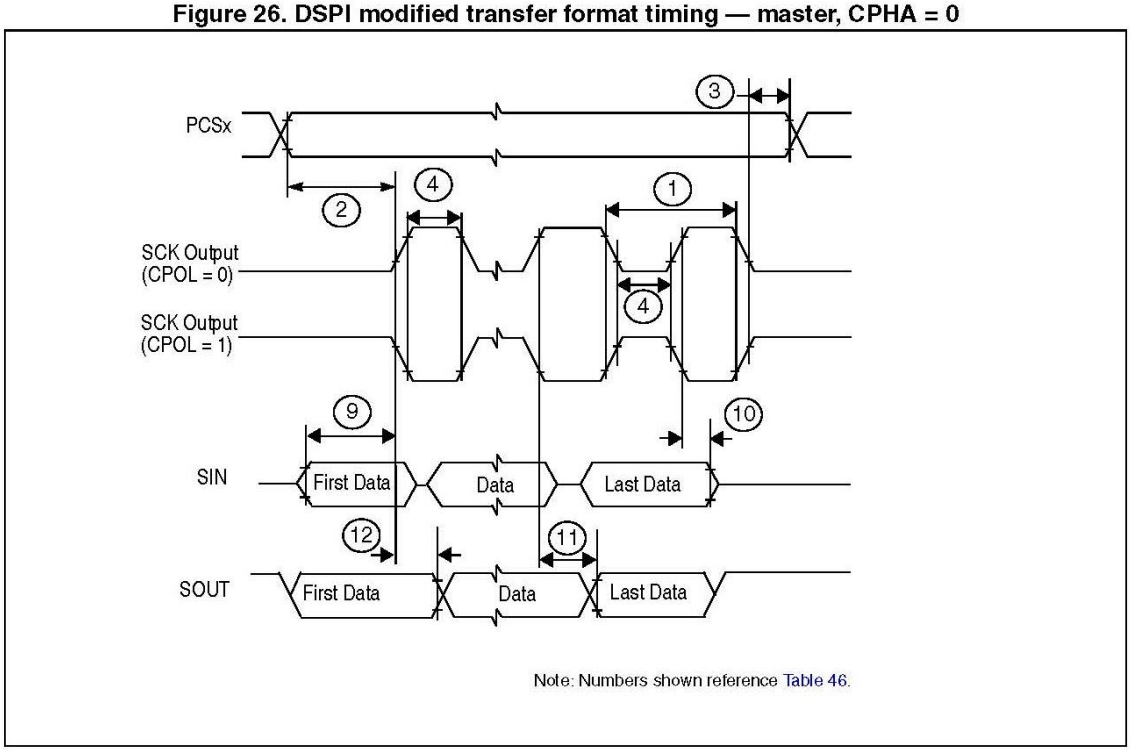


Figure 27. DSPI modified transfer format timing — master, CPHA = 1

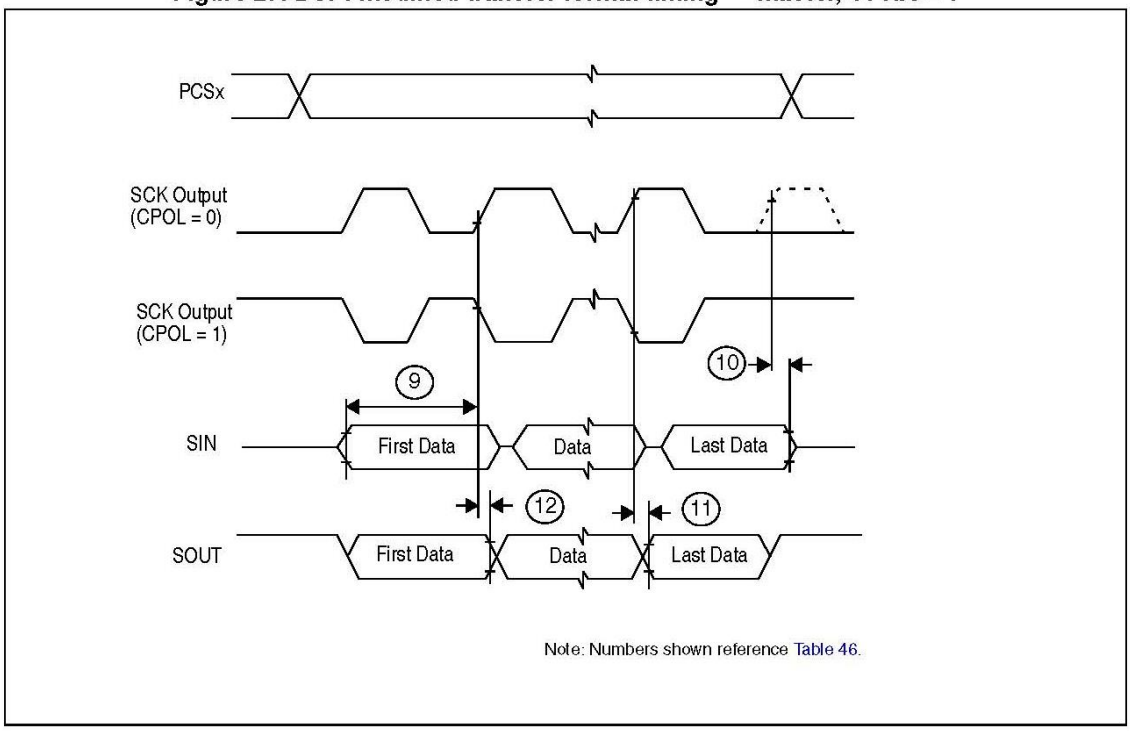


Figure 28. DSPI modified transfer format timing — slave, CPHA = 0

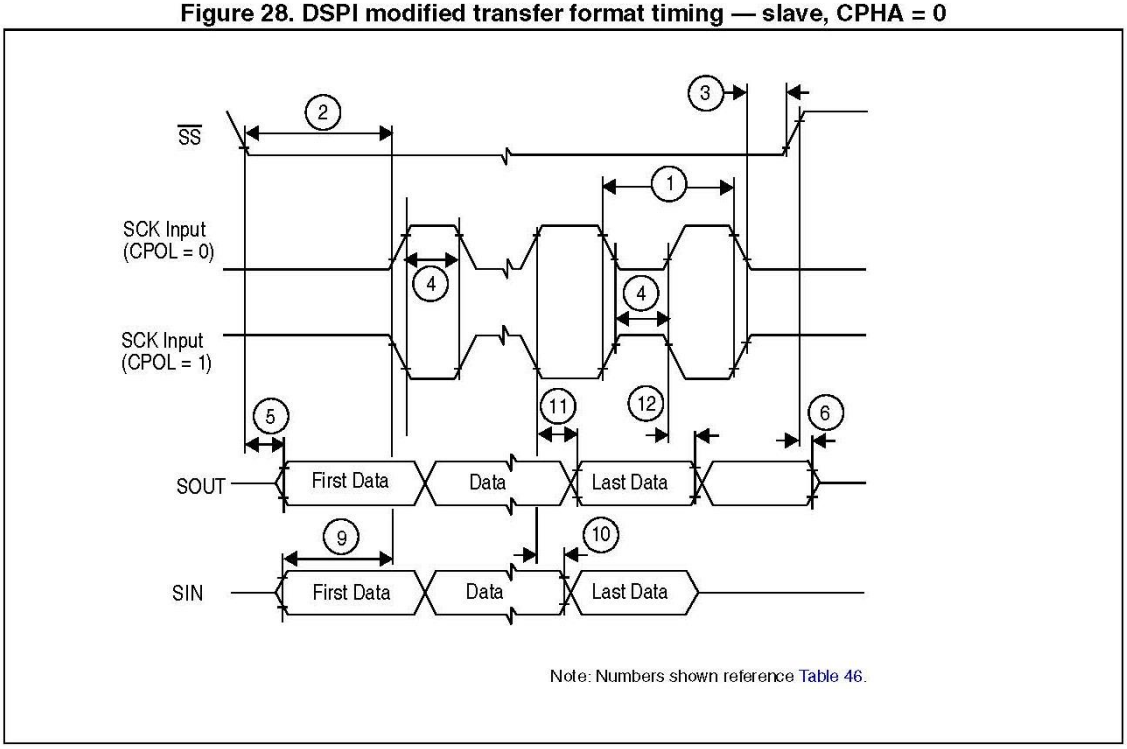
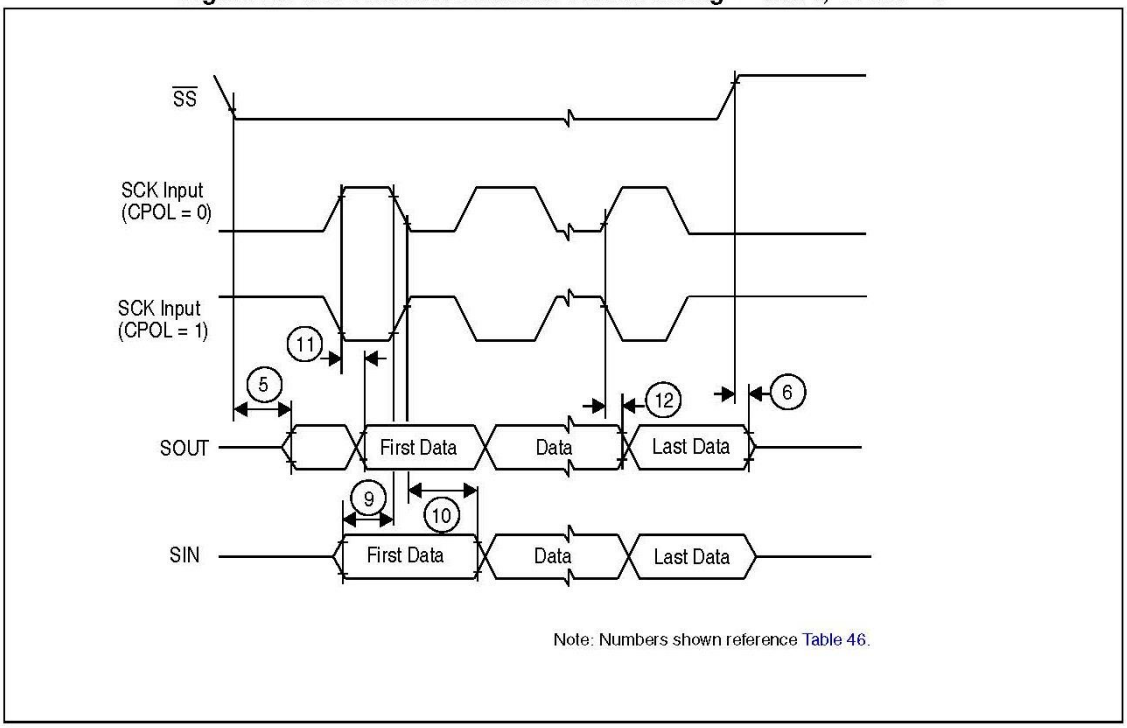
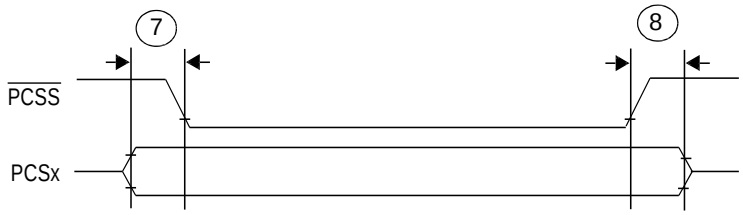


Figure 29. DSPI modified transfer format timing — slave, CPHA = 1





Note: Numbers shown reference Table 46.

Figure 31. DSPI PCS strobe (PCSS) timing

4.17.3 Nexus characteristics

Table 48. Nexus characteristics

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{TCYC}	CC	D	TCK cycle time	64	—	—	ns
2	t_{MCYC}	CC	D	MCKO cycle time	32	—	—	ns
3	t_{MDOV}	CC	D	MCKO low to MDO data valid	—	—	8	ns
4	t_{MSEOV}	CC	D	MCKO low to MSEO_b data valid	—	—	8	ns
5	t_{EVTOV}	CC	D	MCKO low to EVTO data valid	—	—	8	ns
6	t_{NTDIS}	CC	D	TDI data setup time	15	—	—	ns
	t_{NTMSS}	CC	D	TMS data setup time	15	—	—	ns
7	t_{NTDIH}	CC	D	TDI data hold time	5	—	—	ns
	t_{NTMSH}	CC	D	TMS data hold time	5	—	—	ns
8	t_{TDOV}	CC	D	TCK low to TDO data valid	35	—	—	ns
9	t_{TDOI}	CC	D	TCK low to TDO data invalid	6	—	—	ns

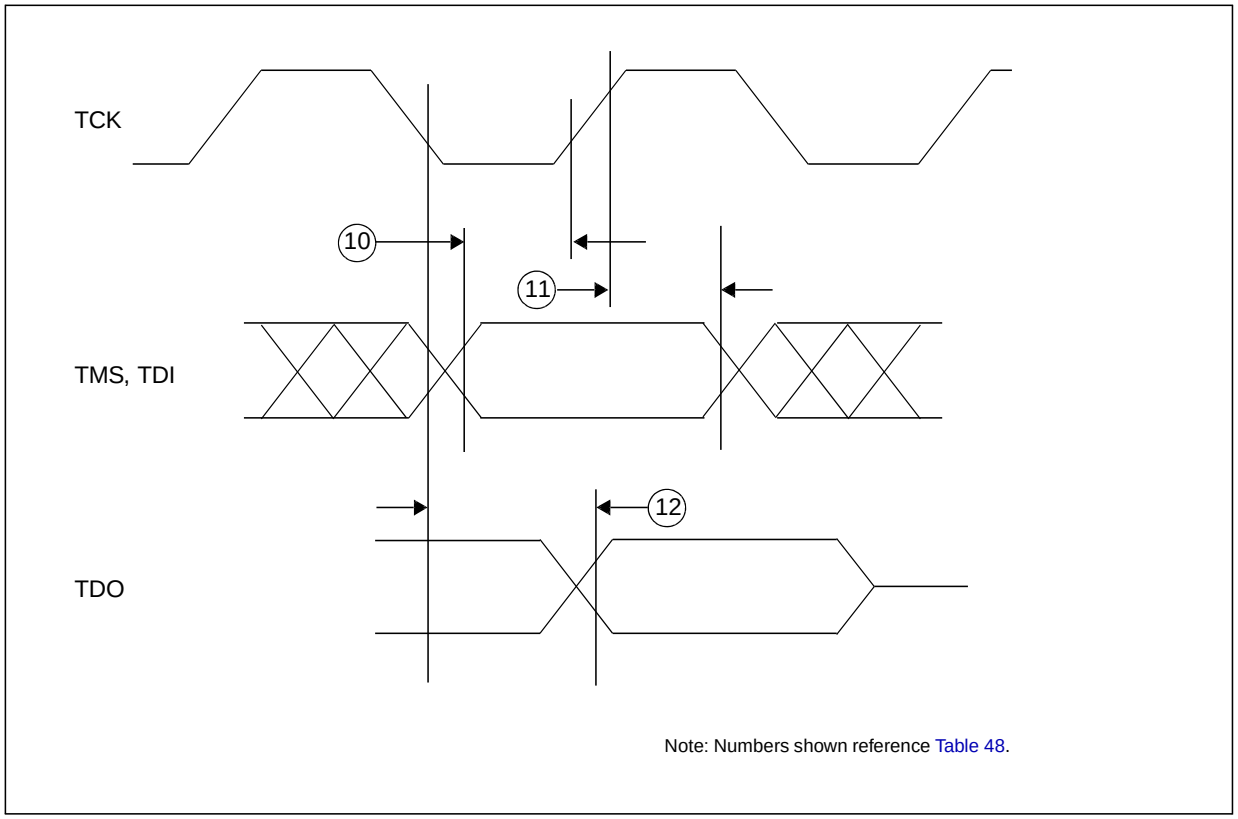


Figure 32. Nexus TDI, TMS, TDO timing

4.17.4 JTAG characteristics

Table 49. JTAG characteristics

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{JCYC}	CC	D	TCK cycle time	64	—	—	ns
2	t_{TDIS}	CC	D	TDI setup time	15	—	—	ns
3	t_{TDIH}	CC	D	TDI hold time	5	—	—	ns
4	t_{TMSS}	CC	D	TMS setup time	15	—	—	ns
5	t_{TMSH}	CC	D	TMS hold time	5	—	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO valid	—	—	33	ns
7	t_{TDOI}	CC	D	TCK low to TDO invalid	6	—	—	ns

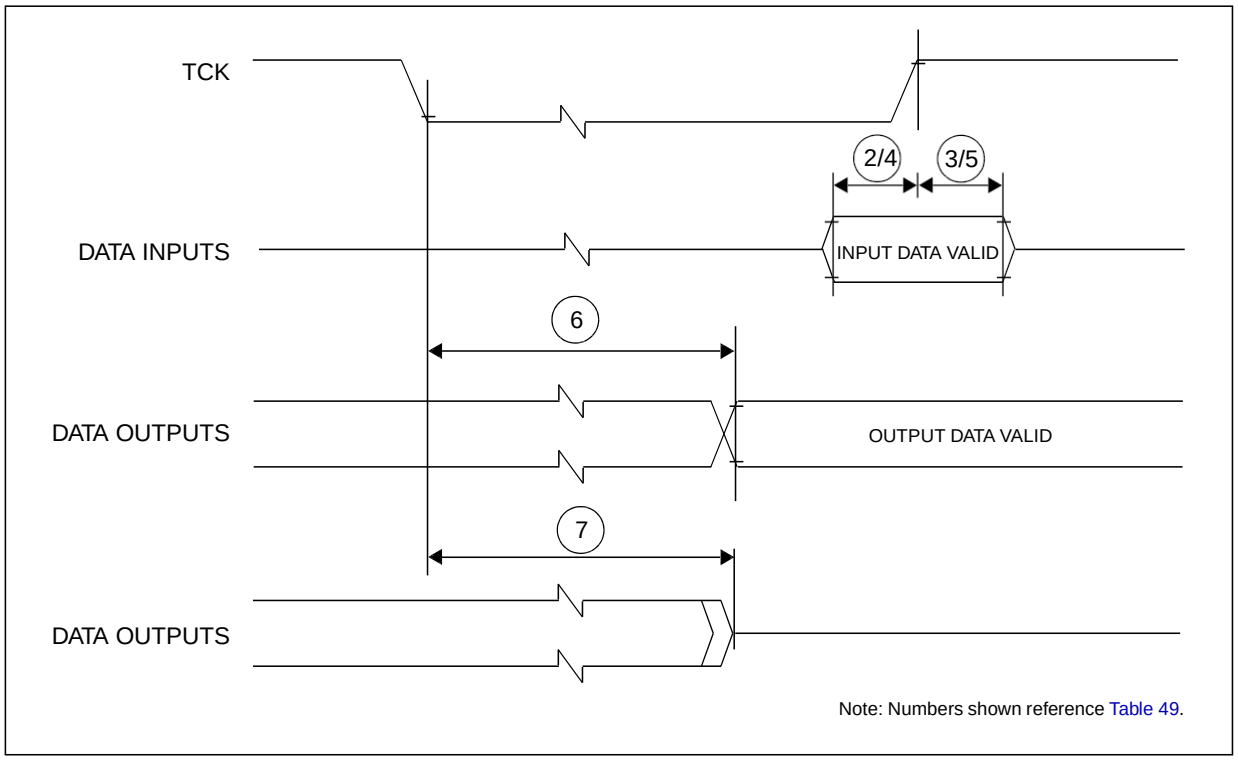


Figure 33. Timing diagram — JTAG boundary scan

5 Differences

This chapter show that points are incompatible with MPC560X. The user should pay attention to:

5.1 CTU

The register can been changed between two different placements described in Figure 29-2.
The mapping of the channel number value to the corresponding ADC channel is provided in Table 29-4-1 or Table 29-4-2. The function can been changed to Table 29- 4- 2 for CCFC2010BC30L5 and CCFC2010BC30L3.

5.2 SRAM

The size of sram in CCFC2010BC30LX is 32Kbyte.

5.3 INTC

Whether the interrupt sources described in Table 18-10 exist actually depends on the existence of the modules in each chip. All interrupt sources above 233 in CCFC2010BC do not exitst on MPC560X.
The hard interrupt vector table's base address has to align with **0x0+0x1000*N** .

5.4 MC_CGM

In Modulation Register (CR) of FMPLL, the formula of INC_STEP is different between CCFC2010BC and MPC560X.
The INC_STEP field is the binary equivalent of the value incstep derived from following formula in CCFC2010BC:

$$\text{incstep} = \text{round}\left(\frac{(2^{10}-1)\times \text{MD}\times \text{EMFD}}{100\times 5\times \text{modperiod}}\right)$$

The INC_STEP field is the binary equivalent of the value incstep derived from following formula in MPC560X:

$$\text{incstep} = \text{round}\left(\frac{(2^{15}-1)\times \text{MD}\times \text{EMFD}}{100\times 5\times \text{modperiod}}\right)$$

The SELCTL in Table 7-4 are different with MPC560X.

SELCTL	CCFC2010BC SERIES	MPC 560X
0000	4-20 MHz ext. xtal osc.	4-16 MHz ext. xtal osc.
0001	16 MHz int. RC osc	16 MHz int. RC osc
0010	freq. mod. PLL	freq. mod. PLL
0011	RTC clock	system clock
0100	128 KHz int. RC osc	RTC clock
0101	system clock	Reserved

5.5 FlexCAN

In addition, the CANFD interface is be support by CCFC2010BC's CAN interface.

5.6 ADC

In ADC5607, INPCMP & INPSAMP in CTR one bit more than MPC560X INPLATCH &OFFSHIFT in CTR is unused. ADC sampling and conversion timing is different from MPC560X Fadc must be less than 16MHz

5.7 PFU

The flash area where 0xFF data has been written to the flash cannot be written to other values. The area can be written only after the flash is erased.
CFLASH size is 256KB in CCFC2010BC30LX.
In CCFC2010BC, PFU registers are different with MPC560X.

Registers	CCFC2010BC SERIES	MPC560X
CFLASH_UT0(User test register)	Not exist	Exists
CFLASH_UT1	Not exist	Exists
CFLASH_UT2	Not exist	Exists
CFLASH_UMISR0(User multiple input signature register)	Not exist	Exists
CFLASH_UMISR1	Not exist	Exists
CFLASH_UMISR2	Not exist	Exists
CFLASH_UMISR3	Not exist	Exists
CFLASH_UMISR4	Not exist	Exists
NVPWD0(Nonvolatile private censorship password register)	Not exist	Exists
NVPWD1	Not exist	Exists
NVSCC0(Nonvolatile system censorship control register)	Not exist	Exists
NVSCC0	Not exist	Exists
DLASH_UT0(User test register)	Not exist	Exists
DLASH_UT1	Not exist	Exists
DLASH_UT2	Not exist	Exists
DLASH_UMISR0(User multiple input signature register)	Not exist	Exists
DLASH_UMISR1	Not exist	Exists
DLASH_UMISR2	Not exist	Exists
DLASH_UMISR3	Not exist	Exists
DLASH_UMISR4	Not exist	Exists

In CCFC2010BC, flash read access timing are different with MPC560X.

Frequency	CCFC2010BC SERIES	MPC560X
80 Mhz	3 wait states	-
64 Mhz	2 wait states	2 wait states
40 Mhz	2 wait states	1 wait state
20 Mhz	2 wait states	0 wait states

5.8 XBAR

Misaligned access is not support in CCFC2010BC. Half word access, the address value must be a multiple of 2. As to word access, the address value must be a multiple of 4.

5.9 MC_ME

Wake up form standby mode, the flash mode of me_drun_mc register(DFLAON&CFLAON) must be configured to 11(normal mode) .

5.10 CLOCK

External crystal oscillator does not need external 1 MΩ resistance.

5.11 DSPI

During DSPI continuous operation, only 10 and 01 modes are supported temporarily, and 00 and 01 mode are not supported in the current version.

5.12 WKUP

When initializing the configuration operation, all wakeup pin in reference manual ***Table 12-1*** need to be configured by pulling up or pulling down, otherwise it will cause electric leakage.

5.13 DMA

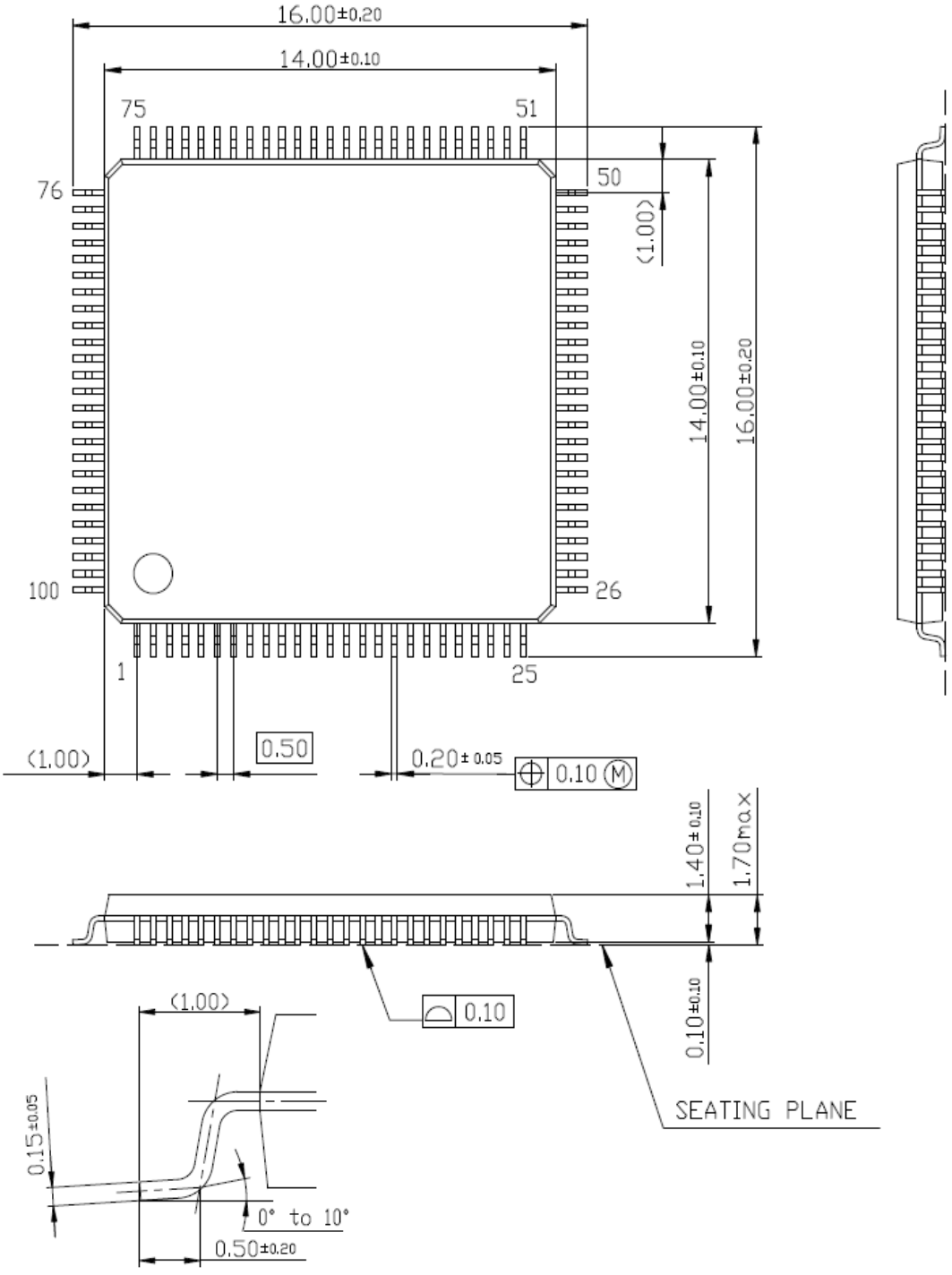
The DMA function is supported by the full range of CCFC2010BC.

6 Package characteristics

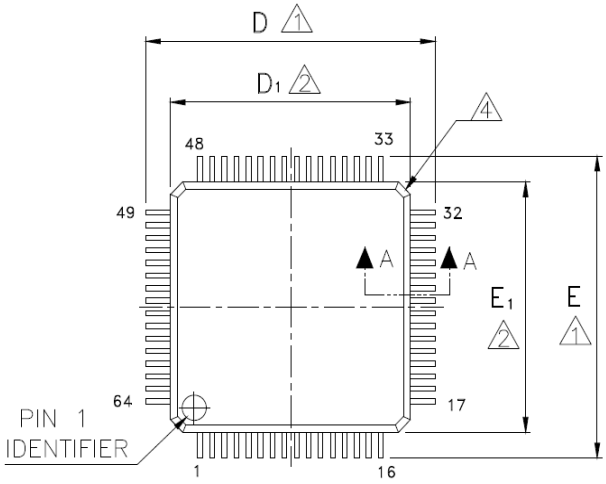
6.1 Package mechanical data

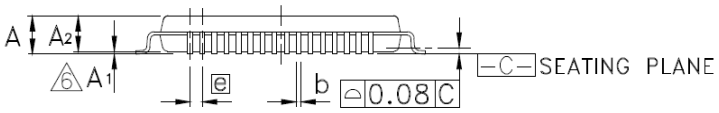
6.1.1 100 LQFP

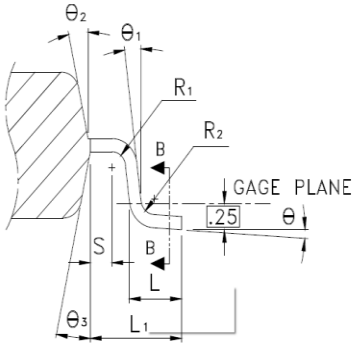
Unit: mm



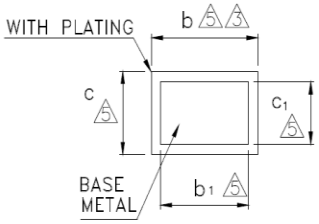
6.1.2 64 LQFP







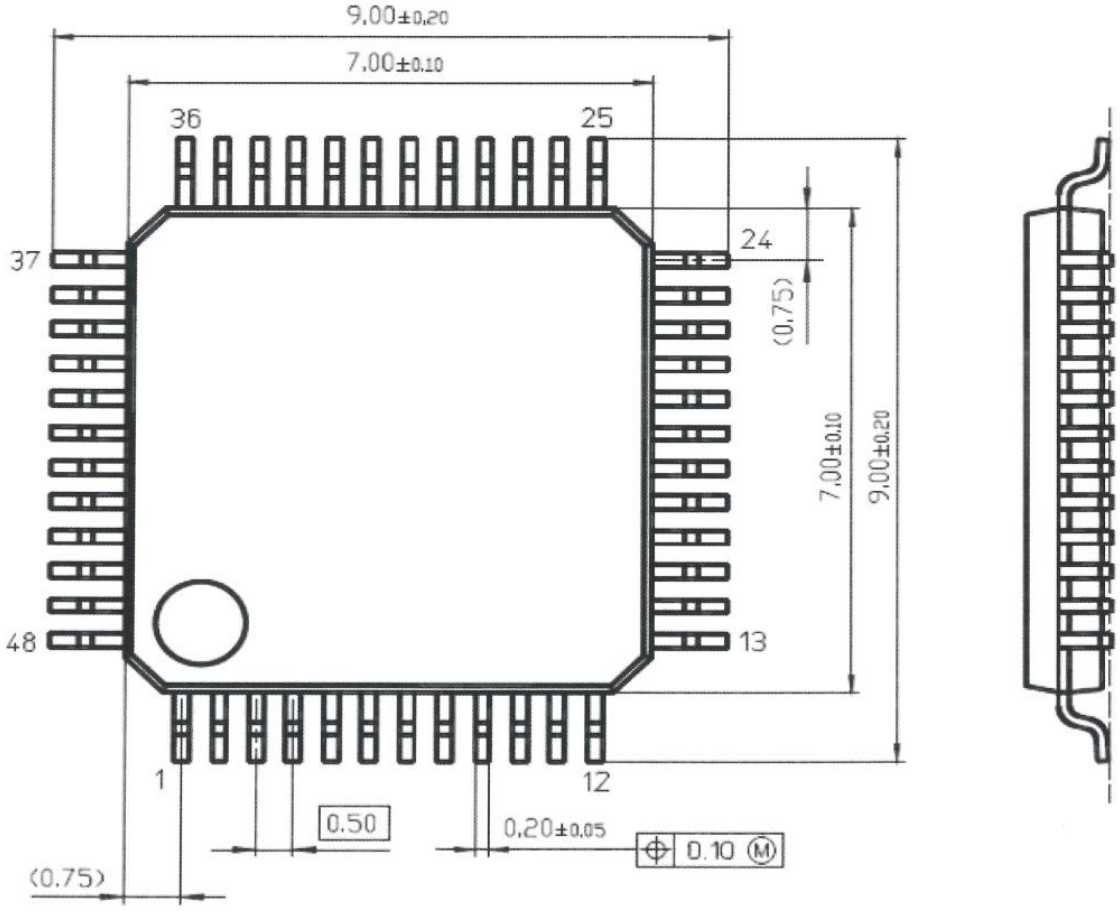
SECTION A–A

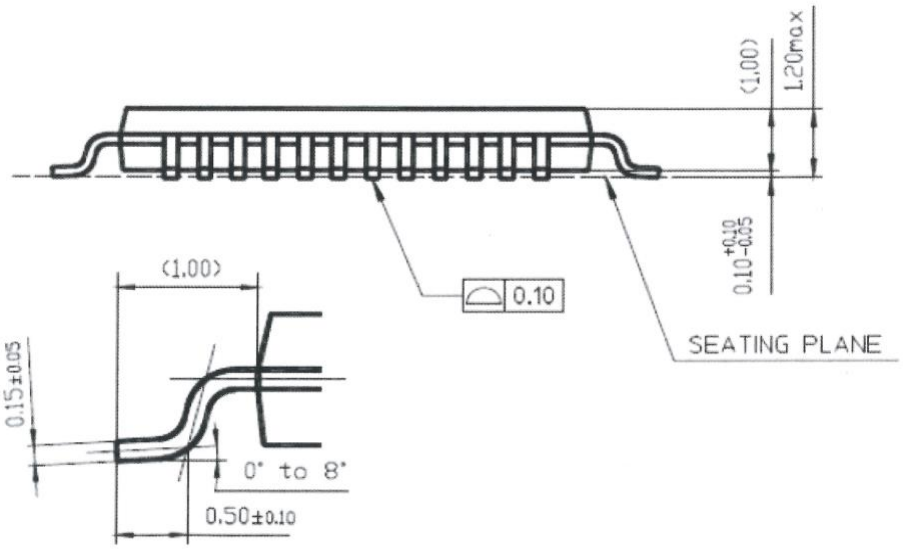


SECTION B–B

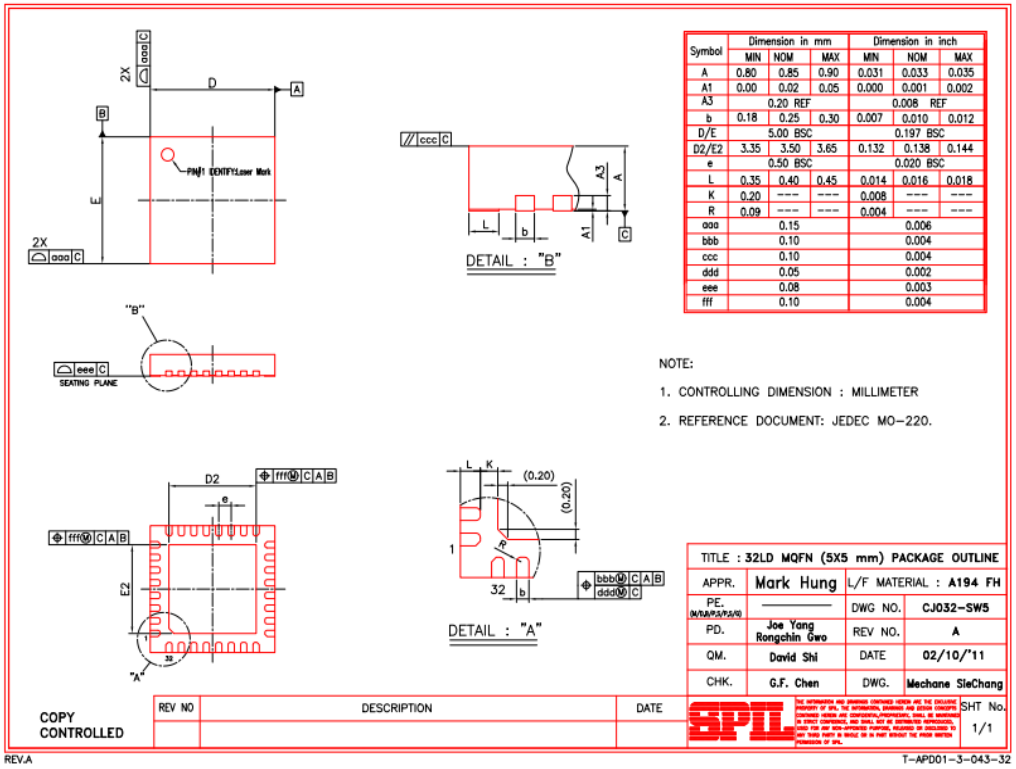
Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.025	—	0.127	0.001	—	0.005
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	12.00 BSC			0.472 BSC		
D1	10.00 BSC			0.394 BSC		
E	12.00 BSC			0.472 BSC		
E1	10.00 BSC			0.394 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	12°TYP			12°TYP		
θ3	12°TYP			12°TYP		

6.1.3 48 TQFP


9.00±0.20
7.00±0.10
36
25
24
37
48
13
1
12
(0.75)
7.00±0.10
9.00±0.20
0.50
0.20±0.05
0.10 M
(0.75)


(1.00)
1.20max
0.10
SEATING PLANE
(1.00)
0.15±0.05
0° to 8°
0.50±0.10

6.1.3 32 QFN



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	5.00 BSC			0.197 BSC		
D2/E2	3.35	3.50	3.65	0.132	0.138	0.144
e	0.50 BSC			0.020 BSC		
L	0.35	0.40	0.45	0.014	0.016	0.018
K	0.20	---	---	0.008	---	---
R	0.09	---	---	0.004	---	---
aaa	0.15			0.006		
bbb	0.10			0.004		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

TITLE : 32LD MQFN (5X5 mm) PACKAGE OUTLINE			
APPR.	Mark Hung	L/F MATERIAL :	A194 FH
PE. (M/TA/P/S/PS/G)	———	DWG NO.	CJ032-SW5
PD.	Joe Yang Rongchin Gwo	REV NO.	A
QM.	David Shi	DATE	02/10/'11
CHK.	G.F. Chen	DWG.	Mechane SieChang

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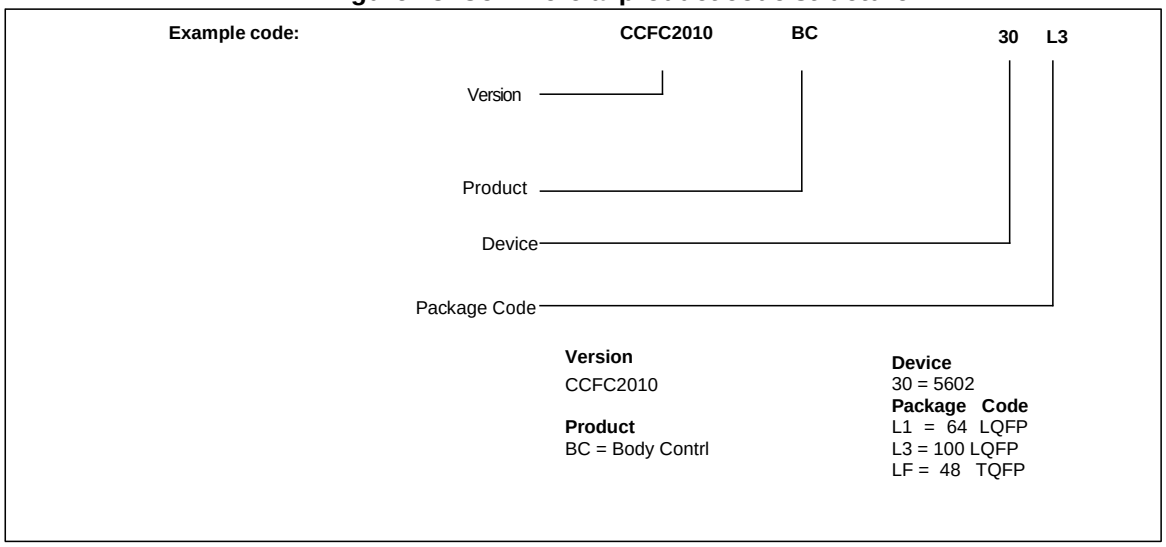
SHT No. 1/1

7 Ordering information

Figure 43. Commercial product code structure



8 Revision history

Table 54 summarizes revisions to this document.

Table 54. Revision history

Revision	Date	Substantive changes
1.0	22-Aug-2022	Initial release(Electrical characteristics shall be subject to the actual measurement)

Appendix A Abbreviations

Table 53 lists abbreviations used but not defined elsewhere in this document.

Table 53.
Abbreviations

Abbreviation	Meaning
CMOS	Complementary metal oxide semiconductor
CPHA	Clock phase
CPOL	Clock polarity
CS	Peripheral chip select
EVTO	Event out
MCKO	Message clock out
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
SCK	Serial communications clock
SOUT	Serial data out
TBD	To be defined
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select